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LETTER

High-Performance Perovskite Single-Junction and Textured Perovskite/Silicon Tandem Solar Cells via Slot-Die-Coating

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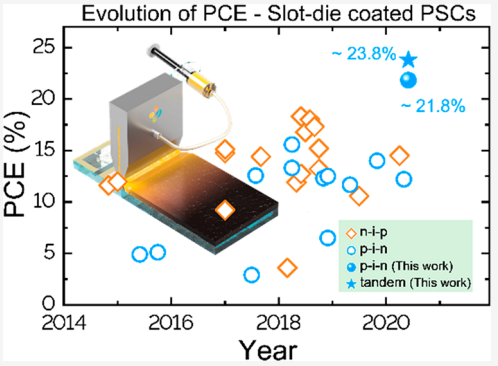
ABSTRACT: **In this work, we report perovskite solar cells in the planar *p*−*i*−*n* configuration based on single-step, anti-solvent-free, low-temperature (70 °C) slot-die-coated methylammonium lead tri-iodide ($MAPbI_3$). The devices are fabricated on hydrophobic poly(triarylamine) (PTAA) surfaces, using key strategies such as solvent engineering, enhanced ink−substrate dynamics, and surface passivation, enabling a power conversion efficiency (PCE) of 21.8%. We also adapted the technique to achieve the first slot-die-coated perovskite/silicon monolithic 2-terminal tandems, achieving a PCE of 23.8% utilizing a textured silicon bottom cell.**



The remarkable progress of hybrid organic−inorganic perovskite solar cells (PSCs) has been enabled by spin-coating of the perovskite absorber, to date.[1] However, the technique is widely considered unsuitable for mass manufacturing. Indeed, the successful commercialization of PSCs demands high-throughput, scalable fabrication techniques with minimal operational expenditure and production costs,[2] thereby motivating the translation of this technology to industrially relevant deposition techniques.[3] In addition to the progress made using vacuum-processed techniques toward large-area devices and modules,[4] various scalable perovskite solution-processing techniques such as blade-coating, slot-die-coating, spray-coating, and inkjet printing have also gathered considerable attention recently.[5,6] Among these techniques, slot-die-coating offers significant advantages in terms of throughput, material utilization, scalability, and the ability to be integrated with sheet-to-sheet and roll-to-roll systems on an industrial level.[7,8]

Recent efforts also aim at integrating perovskites with crystalline silicon (c-Si) as two-terminal (2T), monolithic tandem solar cells, with the reported tandem power conversion efficiencies (PCEs) making progress toward exceeding the single-junction crystalline-silicon (c-Si) efficiency limit.[9,10] Therefore, a scalable perovskite fabrication technique, compatible with integration into a c-Si-based tandem cell, offers significant advantages toward commercialization. To this effect, we sought to develop efficient PSCs using a one-step slot-die-coating technique, with the aim of translating the process to the fabrication of slot-die-coated monolithic perovskite/silicon tandem devices on textured c-Si bottom cells.

To date, small-area (~0.1 cm^2) single-junction slot-die-coated PSCs have resulted in PCEs of 18%,[8,11] but this is still appreciably below the performance of spin-coated devices. Notably, most of these slot-die-based PSCs employ the classic *n*−*i*−*p* device configuration, with binary metal oxides (SnO_2, TiO_2, ZnO) as the electron transport layer (ETL).[8,11−14] Even though recent efforts promise low-temperature process methodologies for these metal oxides,[15−17] a major hurdle for the scalability of *n*−*i*−*p* PSCs is the lack of suitable alternatives to the expensive spiro-OMeTAD (2,2′,7,7′-tetrakis[*N*,*N*-di(4-methoxyphenyl)amino]-9,9′-spirobifluorene) hole transport layer (HTL). However, low-temperature-

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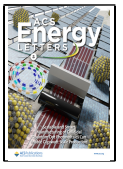
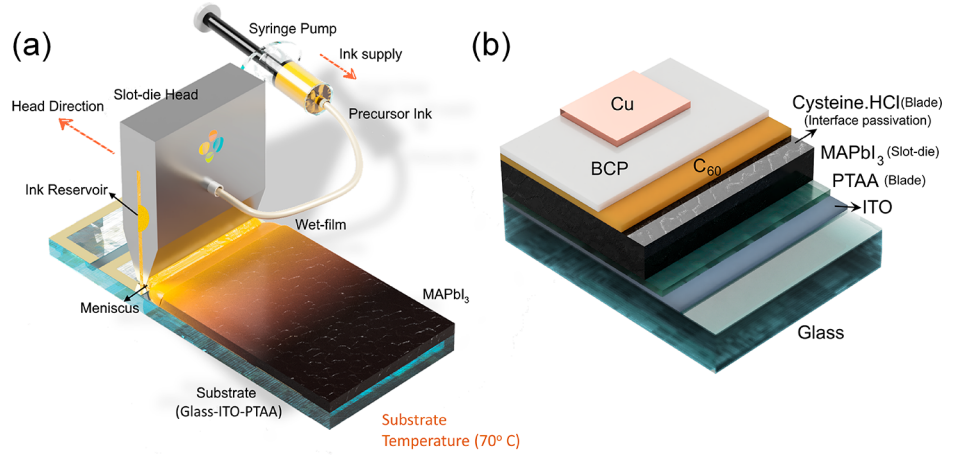


Scheme 1. (a) Slot-Die-Coating Technique and Its Key Parameters for a One-Step Controlled Deposition of $MAPbI_3$ on ITO-PTAA Substrates at 70 °C, and (b) Device Architecture of the Planar $p-i-n$ $MAPbI_3$ Perovskite Solar Cell (ITO-PTAA-$MAPbI_3$(Cys.HCl)-C_{60}-BCP-Cu) Fabricated Using the Slot-Die-Coating



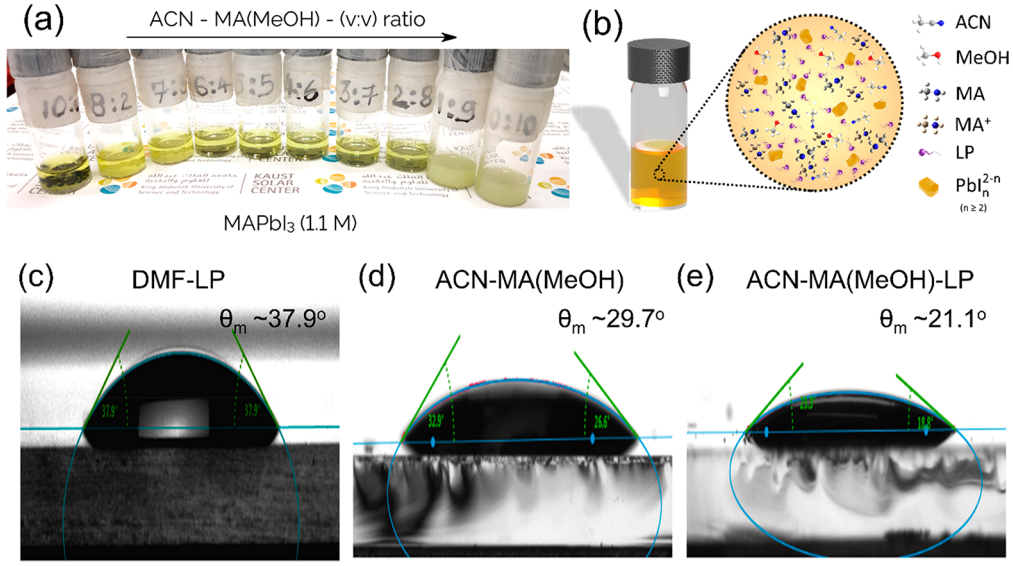


Figure 1. (a) Photograph of precursor solutions composed of 1.1 M $MAPbI_3$ perovskite with varying acetonitrile (ACN) and methylamine (MA) in methanol (MeOH) (40 wt %, commercially available) with different solvent volume ratios (10:0 to 0:10). (b) Illustration of precursor ink constituents used for the one-step slot-die-coating of $MAPbI_3$ on PTAA substrates employed in this study. Contact-angle measurements of 1.1 M $MAPbI_3$ precursor solution on PTAA substrates using (c) DMF solvent with LP additive (L-α-phosphatidylcholine—0.075 wt % of $MAPbI_3$), (d) ACN+MA(MeOH) mixture (6:4), and (e) ACN+MA(MeOH) with LP additive (0.075 wt % of $MAPbI_3$).

processed organic charge transport layers, as already used for organic light-emitting diode fabrication, may be of higher commercial relevance. For the inverted $p-i-n$ device configuration, slot-die-coated PSCs reported in the literature typically employ PEDOT:PSS (poly(3,4-ethylenedioxythiophene) polystyrenesulfonate) as the HTL, resulting in only modest PCEs.[18−20] In contrast, for spin-coated PSCs in the $p-i-n$ configuration, poly(triarylamine) (PTAA) is most commonly used as an HTL, enabling efficient devices.[21] Despite the demonstrated gain in performance from PTAA on spin-coated devices,[22] no report has utilized PTAA for slot-die-coated PSCs.[7] This is due to nonuniform perovskite thin-film formation on the hydrophobic PTAA surface, which hinders the wetting by conventional perovskite inks (mostly based on *N*,*N*-dimethylformamide (DMF) as solvent). Also, the absence of a centrifugal force, inherent to spin-coating, makes slot-die-coating of hydrophilic perovskite inks on hydrophobic PTAA substrates a challenge.[22] Interestingly, recent studies of surfactant-additives facilitated highly efficient $p-i-n$ devices on PTAA substrates via blade-coating at elevated substrate temperatures.[22,23]

Herein, we realize efficient single-step slot-die-coated $p-i-n$ PSCs with hydrophobic PTAA as the HTL (Scheme 1a), via a combination of three key strategies, namely, solvent engineering, surfactant-additives for improved ink-wetting, and interface passivation. The ink−substrate kinetics, the properties of solvents influencing the drying process, and the crystallization rate are key enablers to achieve high-quality slot-die-coated PSCs. First, we translate the $MAPbI_3$ precursor ink from the conventional DMF solvent toward low-boiling-point acetonitrile (ACN) with the addition of a methylamine (dissolved in methanol) (MA(MeOH)) mixture.[24,25] The use of the ACN +MA(MeOH) solvent system dramatically alters the fluid drying dynamics, ensuring swift evaporation of the solvent.

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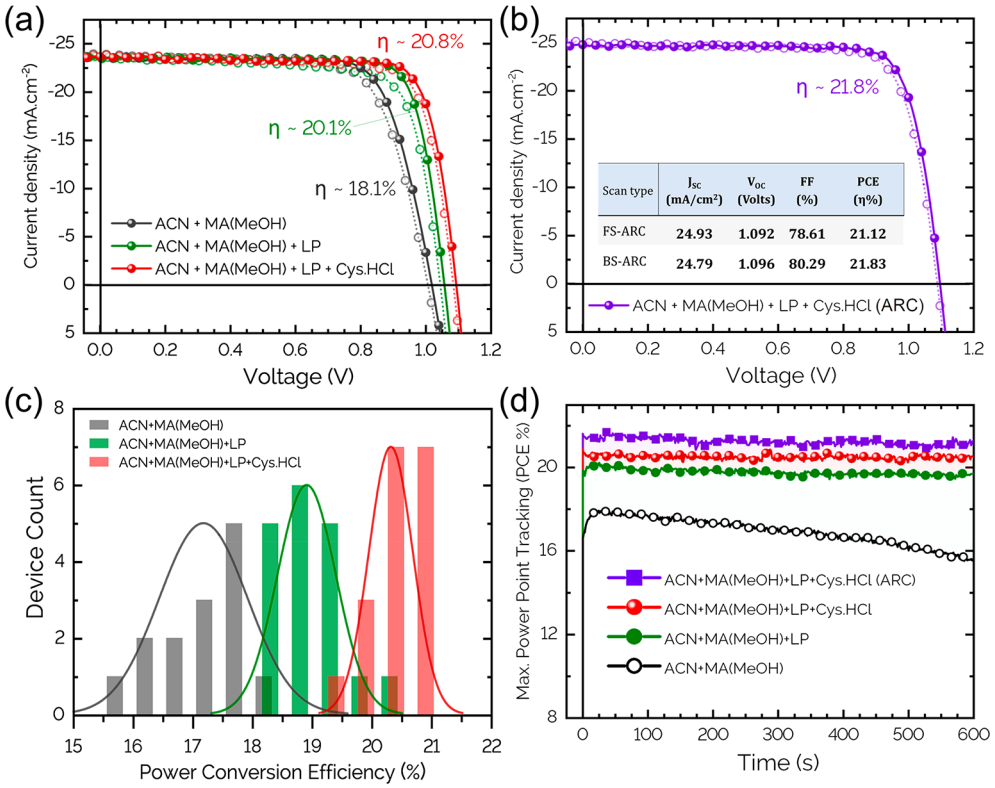

Figure 2. (a) Comparison of *J*−*V* curves of champion slot-die-coated $MAPbI_3$ devices fabricated and optimized using ACN+MA(MeOH) solvent precursor (black), ACN+MA(MeOH) solvent + LP additive (green), and ACN+MA(MeOH) solvent + LP additive followed by Cys.HCl surface treatment via blade-coating (red). (b) *J*−*V* characteristic of the champion slot-die-coated device measured with additional ARF after optimizing the deposition parameters (straight line (sphere) stands for backward scan, and dotted line (circle) depicts forward scan). (c) Distribution statistics of PCE for the corresponding devices fitted to a Gaussian distribution. (d) Maximum power point tracking of the different slot-die-coated devices in this study for 10 min.

Second, we incorporate a surfactant, L-α-phosphatidylcholine (LP, Figure S1), as an additive that leads to better wettability and ink−substrate interaction on hydrophobic PTAA substrates, as reported earlier for DMF-based precursor inks.[22] Third, we passivate the $MAPbI_3$ perovskite surface using cysteine hydrochloride (Cys.HCl, Figure S1) to minimize open-circuit voltage (V_{oc}) losses. Scheme 1b depicts the inverted *p*−*i*−*n* device structure (ITO-PTAA-$MAPbI_3$(Cys.HCl)-C_{60}-BCP-Cu) used in this study. The fabrication of the slot-die-coated PSCs is described in detail in the experimental section (see the SI).

One successful approach to ink development for scalable processing involves replacing polar aprotic solvents with ACN, aided by dissolved MA gas.[24,25] Moving away from the widely used DMF-based precursor inks allows a reduction in substrate temperature from ∼150 °C to as low as ∼70 °C, which is critical to ensure rapid crystallization without antisolvent extraction. We further improve the ease of ink-preparation by using commercially available MA in methanol (∼9.8 mol L^{-1}) with ACN resulting in a stable $MAPbI_3$ precursor ink. Figure 1a shows the $MAPbI_3$ precursor ink with different volume ratios of ACN:MA(MeOH) (0:10 to 10:0) used to dissolve 1.1 M methylammonium iodide (MAI) and lead iodide (PbI_2) precursor salts. Earlier studies dissolve methylamine gas in ACN to form the precursor ink with ACN acting as a primary channel to dissolve the $MA^+PbI_3^-{\cdot}xMA$ perovskite liquid phase. With the use of commercial MA(MeOH), we dissolve the 1.1 M precursor salts using an optimized volume ratio of 600 μL:400 μL (ACN:MA(MeOH)), resulting in a stable, clear solution. Also, higher volumes of MA(MeOH) adversely impact the precursor ink, forming milky dispersions as the presence of polar aprotic ACN is essential to dissolve the precursor constituents. The $MAPbI_3$(ACN+MA(MeOH)) precursor ink is subsequently modified by adding small quantities of LP additive. Figure 1b illustrates the individual components of the precursor ink used for the one-step slot-die-coating of $MAPbI_3$ thin films in this study. The optimizations of ACN:MA(MeOH) volume ratio (6:4) and LP additive concentration (0.075 wt % of $MAPbI_3$) are carried out separately via PSCs made by the blade-coating of $MAPbI_3$, and the corresponding values are adapted for slot-die-coating here.

For the planar *p*−*i*−*n* PSC configuration in this study, first, the hydrophobic PTAA layer is coated on glass-ITO substrates via meniscus-coating. Figure 1c−e compares the contact-angles formed by $MAPbI_3$(DMF+LP), $MAPbI_3$(ACN+MA(MeOH)), and $MAPbI_3$(ACN+MA(MeOH)+LP) inks with the hydrophobic PTAA surface, respectively. Even though the $MAPbI_3$(DMF+LP) ink is known to produce efficient PSCs, the reduction in surface tension is evident from the lower contact-angle made by the $MAPbI_3$(ACN+MA(MeOH)) ink with the hydrophobic surface, even without the LP additive. The addition of LP further reduces the contact-angle of $MAPbI_3$(ACN+MA(MeOH)) ink with the PTAA substrate, resulting in a better wettability and uniform perovskite films. Scanning electron microscope (SEM) images reveal the contrast in the $MAPbI_3$ film quality using the three different inks (Figure S2a−c). Slot-die-coated $MAPbI_3$ films based on the (ACN+MA(MeOH)+LP) ink demonstrate improved grain

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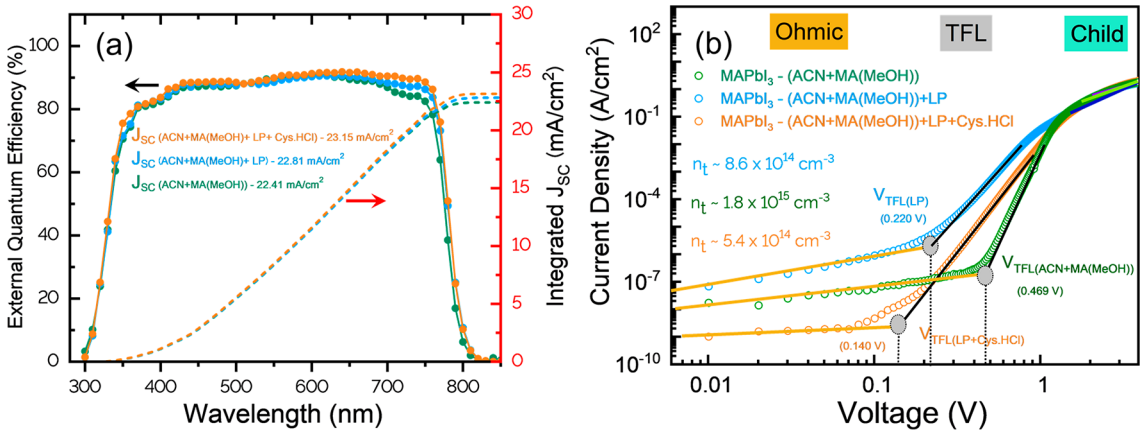

Figure 3. (a) External quantum efficiency (EQE) and integrated short-circuit current-density of slot-die-coated $MAPbI_3$ PSCs fabricated using different precursor solutions, namely, ACN+MA(MeOH) (control), ACN+MA(MeOH) + LP additive (LP), and ACN+MA(MeOH) + LP followed by Cys.HCl passivation (LP+Cys.HCl). (b) Space-charge limited current (SCLC) measurement in the dark showing the $J-V$ traces with three different regimes of operation for slot-die-coated $MAPbI_3$ $p-i-n$ devices fabricated using the different process conditions.

size with seemingly spherulitic domains (Figure S3a) over DMF+LP and ACN+MA(MeOH) inks. Figure S4 shows atomic force microscopy (AFM) images of slot-die-coated $MAPbI_3$ films without and with the LP additive using ACN +MA(MeOH) inks. The incorporation of LP leads to more uniform films, made evident by the greatly reduced root-mean-square (RMS) roughness determined by AFM (Figure S4). Notably, for DMF+LP inks, the slot-die-coating is carried out at 140 °C, whereas for the other two inks, the substrate is only at 70 °C. Figures S2d and S3b illustrate the top-surface SEM image of the $MAPbI_3$ thin films after an interface passivation treatment with blade-coated Cys.HCl (dissolved in IPA). The presence of chlorine allows for the recrystallization of the grains, slightly improving their size (compare Figure S2c,d), and this is also evident from the X-ray diffraction (XRD) measurements (Figure S5). Despite the increase in grain size, the Cys.HCl treated films exhibit a reduced RMS roughness (Figure S4). We expect the $-COOH$, $-NH_2$, and $-SH$ functional groups of the cysteine molecule to passivate the noncoordinated Pb^{2+} and I^- defect states, leading to efficient charge collection.[26] Photoluminescence (PL) intensity and time-resolved PL (TRPL) measurements highlight the substantial improvements in minority carrier lifetime of the $MAPbI_3$ absorber with the addition of LP, followed by Cys.HCl treatment (Figure S6 and Table S1). The cysteine-passivated samples exhibited an average carrier lifetime (τ_{avg}) of 1.6 μs, whereas the pristine samples and samples with the LP additive only have a τ_{avg} of 88 and 757 ns, respectively. The PL emission of $MAPbI_3$ samples slot-die-coated on top of the PTAA HTL is significantly quenched in comparison to the pristine samples.

Figure 2a compares the champion $J-V$ curves of one-step slot-die-coated $MAPbI_3$ PSCs employing the device architecture in Scheme 1b for three different conditions: using the ACN+MA(MeOH) solvent precursor; using the ACN+MA-(MeOH) solvent with LP additive; and using the ACN +MA(MeOH) solvent with the LP additive followed by Cys.HCl surface treatment via blade-coating. The ACN +MA(MeOH)-based $MAPbI_3$ control devices (active area ~0.1 cm^2) exhibit a champion PCE of 18.1% (Figure 2a) with an average value of 16.2 ± 2.1% (Figure S7 and Table S2). Adding optimized concentrations of LP additives with the ACN+MA(MeOH) precursor ink resulted in an improvement in PCE with a champion value of 20.1% (average value ~18.9 ± 0.5%). The major improvements in the champion device parameters compared to the LP-free devices are in V_{oc} (1.02 to 1.05 V) and fill factor (FF, 75.0% to 80.6%). We also observe a similar trend for the average parameter values calculated from a batch of 18 devices each (Figure S7 and Table S2). Two parameters that require a significant balance for slot-die-coating are the coating speed and the ink supply rate. Coupled with the printhead−substrate distance, they play a crucial role in $MAPbI_3$ film thickness control, its coverage, and their RMS roughness (Figure S8). A stepwise variation of the parameter space resulted in an optimal slot-die head-speed of 15 mm s^{-1} and an ink-supply rate of 400 μL min^{-1}. Figures S9−S12 and Tables S3 and S4 illustrate the distribution of device parameter statistics and the champion $J-V$ curves with varying slot-die-coating parameters of slot-die head-speed and ink-supply rate.

Surface passivation of LP-based $MAPbI_3$ thin films using blade-coated Cys.HCl (dissolved in IPA) further enhanced the V_{oc} of slot-die-coated $p-i-n$ devices by 40 mV on average. The surface-passivated slot-die PSCs exhibit a champion PCE of 20.8% (20.3 ± 0.36%) (Figure 2a,c) with a V_{oc} of 1.09 V (1.09 ± 0.01 V), short-circuit current-density, J_{sc}, of 23.53 mA cm^{-2} (23.18 ± 0.36 mA cm^{-2}), and FF of 80.9% (80.77 ± 0.9%) (Figure S7 and Table S2). The addition of LP and the introduction of Cys.HCl result in an overall systematic improvement in device parameter distribution for the slot-die-coated PSCs (Figure 2c and Figure S7). These devices set a benchmark for efficient slot-die-coated small-area PSCs and demonstrate the promise of this technique. Introducing a textured antireflective foil (ARF) on the glass superstrate results in a champion slot-die-coated PSC with a PCE of 21.8% (Figure 2b). The enhancement in J_{sc} for the ARF-coated device is attributed to the reduced reflectance of the entire device stack (Figure S13a). Figure S13b shows the corresponding improvement in external quantum efficiency (EQE) measurements. Figure 2d shows the evolution of the maximum power point (MPP) tracked over 600 s with the passivated PSCs exhibiting significantly better stability in comparison to ACN +MA(MeOH) ink-based control samples.

Figure 3a shows the variation in EQE spectra for the average slot-die-coated devices fabricated using the different techniques discussed here. The integrated J_{sc} values calculated from the EQE measurements align well with the average J_{sc} values

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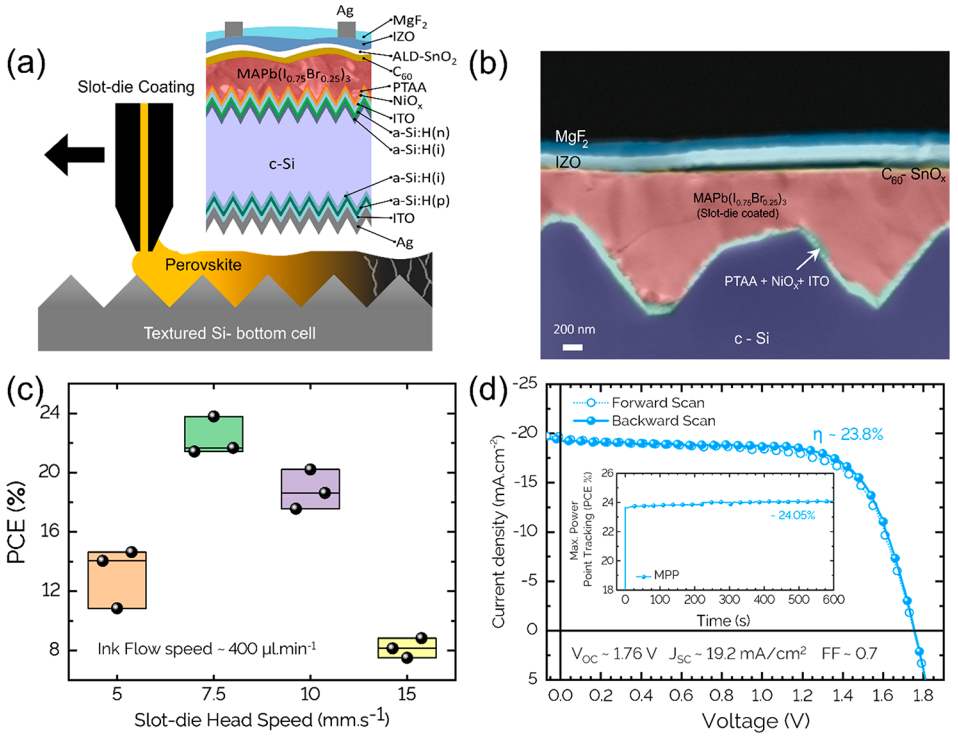

Figure 4. (a) Device architecture schematic of perovskite/silicon tandem devices wherein the wide-band-gap perovskite absorber layer ($MAPb(I_{0.75}Br_{0.25})_3$ ~ 1.68 eV) is deposited by slot-die-coating. (b) Cross-section SEM image of the textured perovskite/silicon tandem device obtained from optimized slot-die-coating parameters. (c) Statistics of PCE of slot-die-coated tandems for different slot-die head-speeds with ACN+MA(MeOH) solvent + LP additive followed by Cys.HCl surface treatment. (d) *J*–*V* curve of champion slot-die-coated perovskite/silicon tandem device (inset: MPP tracking of PCE for 10 min).

measured using *J*–*V* measurements for these devices. The most significant improvement in EQE is seen for the wavelength range 650–800 nm for devices with the LP additive followed by Cys.HCl passivation. This suggests an enhancement in $MAPbI_3$ absorber quality, as observed earlier from PL, TRPL, and SEM measurements, resulting in efficient charge collection. Figure 3b shows the space-charge limited current (SCLC) measurements for the slot-die-coated PSCs. The decrease in onset voltage (V_{TFL}) of the trap-filled limit (TFL; a regime wherein the trap-states are filled by the injected carriers) indicates a reduced trap-density in Cys.HCl treated devices in comparison with the other two devices. The trap-densities of slot-die-coated $MAPbI_3$ *p*–*i*–*n* PSCs based on ACN+MA(MeOH), ACN+MA(MeOH)+LP, and ACN+MA-(MeOH)+LP+Cys.HCl processes are estimated to be 1.8×10^{15}, 8.6×10^{14}, and 5.6×10^{14} cm^{-3}, respectively. The improvement in device parameters for Cys.HCl treated devices is consistent with a decrease in the trap-density estimates. Making use of the slot-die-coating technique, we fabricated minimodules with an active area of 6.8 cm^2 (4 subcells with individual area of 1.7 cm^2) with an actual J_{sc} of 20.53 $mA.cm^{-2}$ (actual current 34.9 mA, and for PCE calculations we use ~5.13 $mA.cm^{-2}$ (~34.9 mA/6.8 cm^{-2})), V_{OC} of 4.05 V, and FF of 0.695 leading to a PCE of 14.4%. Figure S14 summarizes the champion *J*–*V* curves of the slot-die-coated minimodule with the device parameter distribution of 9 devices.

Recent progress on perovskite/silicon tandem devices using solution-processing on textured silicon bottom cells motivates the extension of our technique toward obtaining efficient slot-die-coated tandems.[27,28] Here, we employ a textured silicon heterojunction bottom cell (as reported by Hou et al.[27]) with the perovskite absorber layer deposited by slot-die-coating, using the ACN+MA(MeOH)+LP-based precursor ink followed by Cys.HCl passivation. As in our single-junction PSCs, the polarity of the tandem device is in the *p*–*i*–*n* configuration. The band gap of the absorber material is tuned by incorporating bromine ($MAPb(I_{0.75}Br_{0.25})_3$) to ensure a perovskite band gap of 1.68 eV, required for current-matching. Figures S15–S17 illustrate the UV–vis absorption measurements, SEM top-surface, and XRD pattern of slot-die-coated ($MAPb(I_{0.75}Br_{0.25})_3$) films using the different conditions elucidated earlier. Figures S18 and S19 summarize the performance of the corresponding slot-die-coated single-junction devices for the wide-band-gap absorber. Figure 4a,b represents the device schematic and SEM cross-section of the optimized tandem, respectively. Figure 4c illustrates the variation of PCE with slot-die-coating speed to achieve optimized perovskite/silicon tandems. At a lower slot-die head-speed of 5 mm s^{-1}, a thick perovskite layer is coated on top of the textured Si bottom cell, resulting in inefficient charge collection and performance losses. Relatively higher coating speeds (10–15 mm s^{-1}) yielded uncovered Si pyramids with shunt paths that adversely affected the tandem devices. Figure S20 shows the cross-section SEM images of perovskite/silicon tandems for different slot-die-coating speeds. The tandem devices fabricated with an optimized head-speed of 7.5 mm s^{-1} achieve a better device performance due to the uniform perovskite coverage on top of the Si pyramids over a large area (Figure S21). Figure S22 illustrates the distribution of tandem device parameter statistics for the different process conditions with significant variations arising from V_{oc} and FF. Figure 4d shows the *J*–*V* curve of the champion device (active area ~1 cm^2) exhibiting a PCE of 23.8% (stabilized MPP ~ 24.05%) with a V_{oc} of 1.76 V, J_{sc} of 19.2 mA cm^{-2}, and FF of 0.70.

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Figures S23 and S24 show the EQE of the individual subcells of the perovskite/silicon tandem and the MPP tracking of the champion tandem device for 600 s, respectively. This work represents a proof of concept that demonstrates efficient textured monolithic 2T perovskite/silicon tandem devices using slot-die-coating.

In summary, we systematically enhance the champion performance of slot-die-coated PSCs from 18.3% in the current literature to 21.8% for our champion devices, thereby bringing slot-die-coated PSCs closer to the state-of-the-art spin-coated devices. Table S5 compares the champion performance of slot-die-coated PSCs in the current literature with this work. Importantly, we make use of hydrophobic PTAA substrates for slot-die-coated PSCs in the inverted $p-i-n$ architecture, in contrast to the slot-die PSC reported in the literature, which typically employs PEDOT:PSS as the HTL. This allowed us to reduce the performance gap between spin-coated (23%) and slot-die-coated (21.8%) $p-i-n$ devices. Extending our fabrication technique, we introduce the very first slot-die-coated textured perovskite/silicon, 2T-monolithic tandems with a champion PCE of ∼23.8%. Our results illustrate the promise of slot-die-coating for the scale-up of perovskite solar cells in both their single and multijunction implementations.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsenergylett.0c01297.

Details of material characterization, experimental section, slot-die parameter optimization of devices, literature review of the current state of slot-die-coated PSCs, and additional figures including structures, SEM images, AFM images, XRD patterns, photoluminescence emission spectra, TRPL measurements, device parameter distributions, thin-film thickness distribution, RMS roughness distribution, $J-V$ curves, UV−vis measurements, EQE and J_{sc} values, and maximum power-point tracking measurement (PDF)

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Author Contributions

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Notes

The authors declare no competing financial interest.

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