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Rapid characterization of efficient system level ESD protection strategy using coupling transfer function

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ABSTRACT

This study details a new technique for the fast and efficient design and analysis of system level electrostatic discharge (ESD) protection strategy using developed coupling transfer impedance function. The transfer coupling characteristics from the zapping point to the victim location on a DUT can be computed using coupling transfer gain function. Subsequently, it is integrated with an ESD current source in a SPICE type circuit simulator for the fast and efficient analysis of induced ESD coupling noise and the design of the appropriate ESD protection scheme with the suitable choice of ESD protection device (diodes, SCR, GGNMOS, GCNMOS etc.). The study discusses the different protection schemes i.e. primary, secondary and double ESD protections, and the effect of the selected diode types and ESD stressing levels on the employed protection strategy. The proof-of-concept is validated through the rapid design of suitable system level ESD protection strategy for a microstrip-line PCB, high-speed mobile device memory module, and a portable notebook motherboard.

1. Introduction

The higher data rate needs of the fifth generation (5G), internet of things (IoT), and 4th industrial revolution devices require high-speed semiconductor electronic devices. The placement and connectivity of huge number of ultra low power high-speed micro electronic devices in a close proximity makes them more vulnerable towards the electromagnetic emission/susceptibility and electrostatic discharge (ESD) noises [1,2]. Also, the thickness and area of the semiconductor active elements have seen substantial reduction in recent times which makes the integrated circuits (ICs) more prone to the ESD damages [3–5].

ESD damages can become extremely costly especially for the cases when the faulty undetected damage component is installed at the end user product [6]. The basic level of ESD hardening in ICs and microelectronic devices can be achieved at the design level by incorporating the printed circuit boards layout precautions, installation of decoupling capacitors, and integration of protection networks [4,7,8]. However, depending on the application requirement of device, additional complementary on/off chip ESD protection can be added at the apparatus or PCB level [9,10].

The usual practice for the design of appropriate ESD protection scheme is the ESD susceptibility analysis using full wave EM simulation of the devices [11–13] or the analysis of the induced coupling or current distribution through measurements [14]. The analysis of the effect of the employing various protection strategies on the coupling ESD noise either demands high computational resources with extensive 3D modeling of complex device under test (DUTs) using [11–13] methods or the manufacturing and subsequent testings of each DUT sample with employed ESD protection device as proposed in Ref. [14]. The accurate analysis using full wave modeling methods [11–13] also requires the complete detailed modeling of complex DUTs (like high speed DRAM memory modules, motherboard, and mobile devices *etc.*). These approaches makes the analysis of a suitable ESD protection design of a DUT time-consuming, computationally in-efficient, tedious and expensive.

In this study, we present an efficient and rapid way for the assessment of the intended system level ESD protection scheme for a high speed microelectronic as illustrated in Fig. 1. The proposed method

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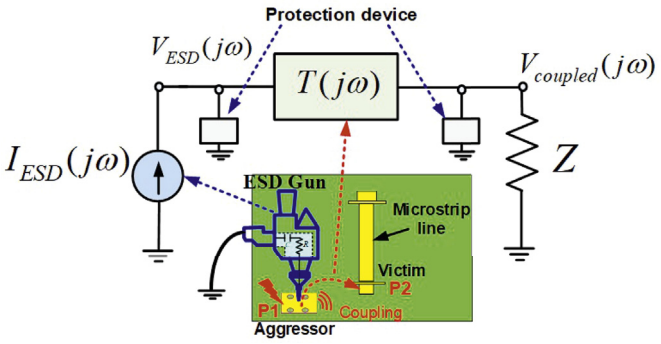

Fig. 1. Proposed strategy for the fast and efficient design of ESD protection scheme.

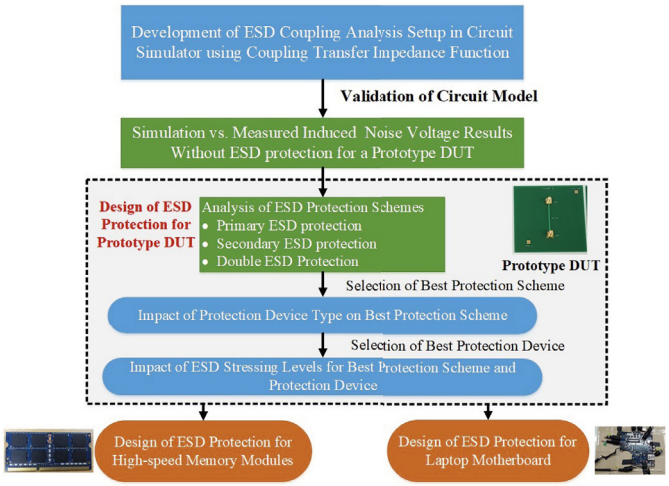

Fig. 2. Analysis framework for fast and efficient design of ESD protection.

involves the fast evaluation of the employed ESD protection strategy in circuit simulator by installing the desired ESD protection device in circuit schematic and checking of its impact on the DUT susceptibility for the injected ESD stressing levels as per the analysis framework of Fig. 2. The transfer coupling characteristics in terms of the coupling transfer impedance function ($T(j\omega)$) from the ESD stressing point (P1) to the victim location (P2) can be computed either through one time full-wave EM simulation or through measurements [15]. The ESD excitation $I_{ESD}(j\omega)$ is modeled as the circuit model of the ESD generator as per the IEC 61000-4-2 requirements [6,16,17]. The circuit modeling of ESD source provides ease for the rapid change in the ESD zapping levels for the analysis of ESD susceptibility of DUT as per IEC requirements [6]. After the validation of the developed circuit model for the ESD coupling analysis, the desired ESD protection device (diodes, SCR, GGNMOS, GCNMOS etc.*etc.*) can be inserted directly in circuit simulator either in component or in a specific SPICE model form. The SPICE model of various commercial ESD protection devices can be obtained from the vendor websites. The proposed procedure of Fig. 1 is validated through the fast design of ESD protection schemes for a designed prototype microstrip line printed circuit board (PCB), high-speed commercial mobile device memory units (DRAM modules), and an operating motherboard of a commercial notebook as illustrated in analysis framework of Fig. 2.

The quick evaluation of different system level testing protection devices makes the ESD protection analysis easy. After the identification of the suitable protection device which reduces the ESD coupling noise significantly till the acceptable level using the proposed strategy, the DUT with that protection device can be manufactured for the subsequent verification. This also makes the overall ESD protection analysis procedure inexpensive with significant reduction in associated ESD protection design analysis cost as compared to Refs. [11–14] methods.

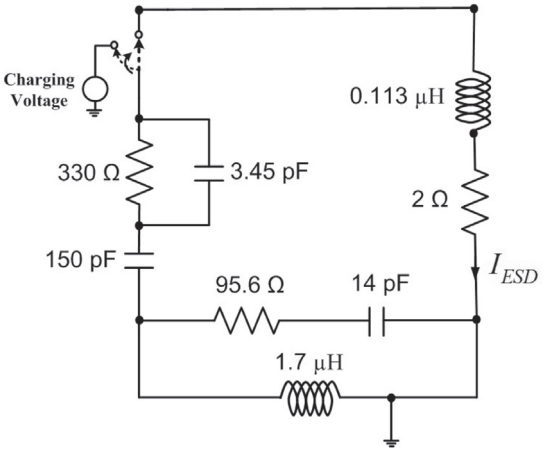

Fig. 3. Circuit model of ESD generator [16,17].

The rest of study is organized as follows: Section 2 briefly explains the procedure for the development of the coupling transfer impedance function and modeling of ESD source for ESD coupling analysis in circuit simulator. The design of various kinds of ESD protection schemes, effect of protection device and ESD stressing levels on protection scheme is discussed in Section 3. Section 4 and 5 discuss the design of ESD protection scheme for the high-speed DRAM memory modules and an operating notebook motherboard. Last Section 6 concludes the study.

2. ESD induced coupling analysis with coupling transfer impedance function

This section briefly explains the procedure of the system level ESD coupling analysis using coupling transfer impedance function [15,17,18] as illustrated in Fig. 1. The ESD coupling transfer impedance function can be determined by converting the simulated or measured two-port *S*-parameters between the zapping point (P1) and victim location (P2), to ABCD form [15]. The induced voltage at the victim location (P2) can then be calculated by using (2) [15]. More details about the determination of the coupling transfer impedance function can be found in Ref. [15].

$$V_{coupled} = T(j\omega)^{-1} I_{ESD}$$
$$where\ T(j\omega) = C + \frac{D}{Z_{load}} \quad (1)$$

The used circuit model as the ESD source is shown in Fig. 3 [16,17]. For the demonstration of the proposed procedure of efficient design of ESD protection strategy and validation of the developed circuit model for the ESD coupling analysis, firstly a prototype microstrip line PCB was designed and fabricated. Fig. 4 shows the schematic and fabricated model of the prototype microstrip line PCB. The length and width of the microstrip trace are 50 mm and 1 mm respectively. After that the procedure is extended for the characterization of commercial DRAM memory modules and a real operating notebook motherboard (details in Sections 4 and 5).

As per the analysis framework of Fig. 2, prior to the design of ESD protection scheme, the validation of Fig. 1 setup is performed by comparing the simulated and measured results of the induced ESD noise at the victim location of Fig. 4 DUT. Fig. 5 shows the measurement setup for the time-domain and frequency domain measurements of the fabricated μ-strip line PCB. The actual time domain and frequency domain experiment pictures are shown in Fig. 6. The ESD gun is used to zap

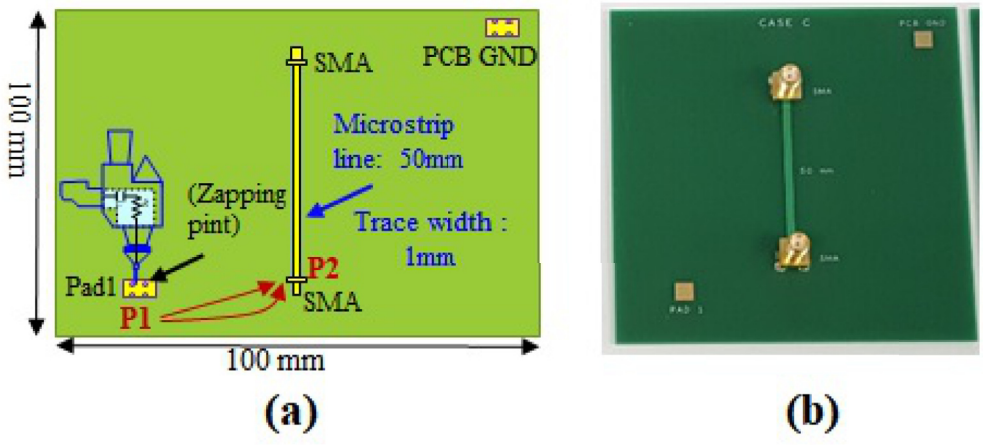

Fig. 4. Prototype microstrip line printed circuit board (PCB): (a) Schematic (b) Fabricated model.

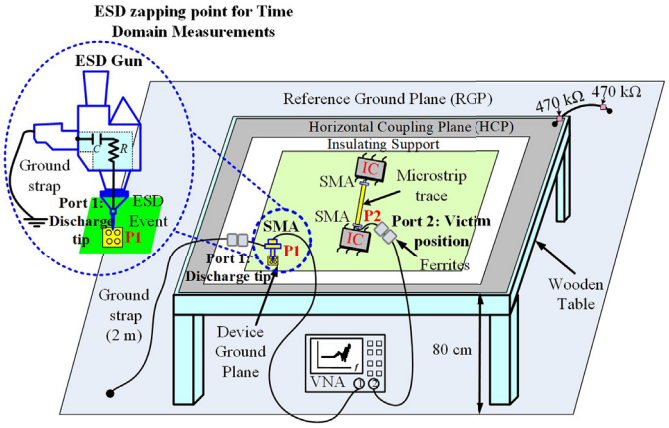

Fig. 5. Frequency domain measurement setup for the computation of coupling transfer impedance function.

the ground plane of the PCB (P1) and the induced voltage at the victim location (P2) on the microstrip line PCB is recorded using an oscilloscope as illustrated in Fig. 6 (a). For the *S*-parameter measurements, ESD gun was replaced with a mocked SMA connector at the zapping location (P1) and the two-port *S*-parameters were recorded between the zapping point (P1) and the victim location (P2) [15] as illustrated in Figs. 5 and 6(b) respectively.

The comparison of measured and simulated induced ESD voltages at the victim location of the μ-strip line PCB for four different ESD zapping levels is shown in Fig. 7. The simulated waveforms are computed in Advance Design System (ADS) circuit simulator using (2) for the four different ESD current waveforms as input (obtained using Fig. 3) corresponding to the ESD discharge voltage levels of +2 kV, +4 kV, +6 kV and +8 kV. The good degree of agreement between the simulated and measured waveforms validates the proposed strategy of ESD coupling analysis of Fig. 1. It deduces that the developed induced coupling analysis strategy in circuit simulator based on the coupling transfer impedance function for the micro-strip line PCB can be used as an authentic model for onward analysis. This developed model is then used for the designing of an efficient ESD protection scheme for the reduction of the induced ESD noise from the aggressor point (P1) to the victim point (P2) for the same μ-strip line PCB, DRAM memory modules and a laptop motherboard.

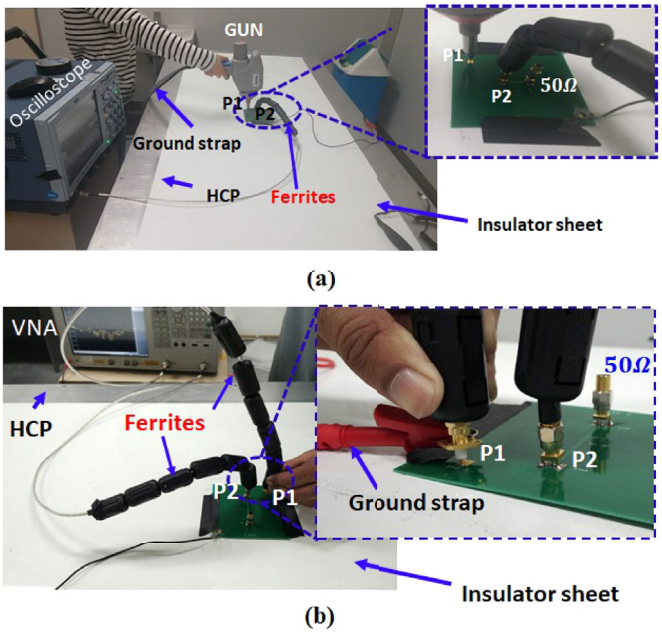

Fig. 6. Measurement setup for the ESD coupling analysis of μ-strip line PCB; (a) Time domain setup for ESD coupling analysis (b) Frequency domain setup *S*-parameter measurements.

3. Design of ESD protection scheme for microstrip line PCB

This sections illustrates the analysis of the design of different kind of ESD protection schemes using various kinds of protection devices for the minimization of the coupled ESD noise at the victim location of a device.

The circuit simulated induced voltage results for the prototype DUT of Fig. 4 computed using proposed coupling analysis strategy of Fig. 1 are shown in Fig. 8 for the +2 kV ESD stressing level. Fig. 8 (a) shows the input voltage level at the source point (i.e. V_{ESD}) while the coupled voltage result for a 50 Ω load is illustrated in Fig. 8 (b). It can be observed from Fig. 8 (a) that the input voltage level for the input ESD current of +2 kV is quite high (≈500 V). The corresponding maximum and peak to peak (PP) induced voltage levels at the load end are 0.62 V and 1.80 V as shown in Fig. 8 (b) without any system level ESD protection.

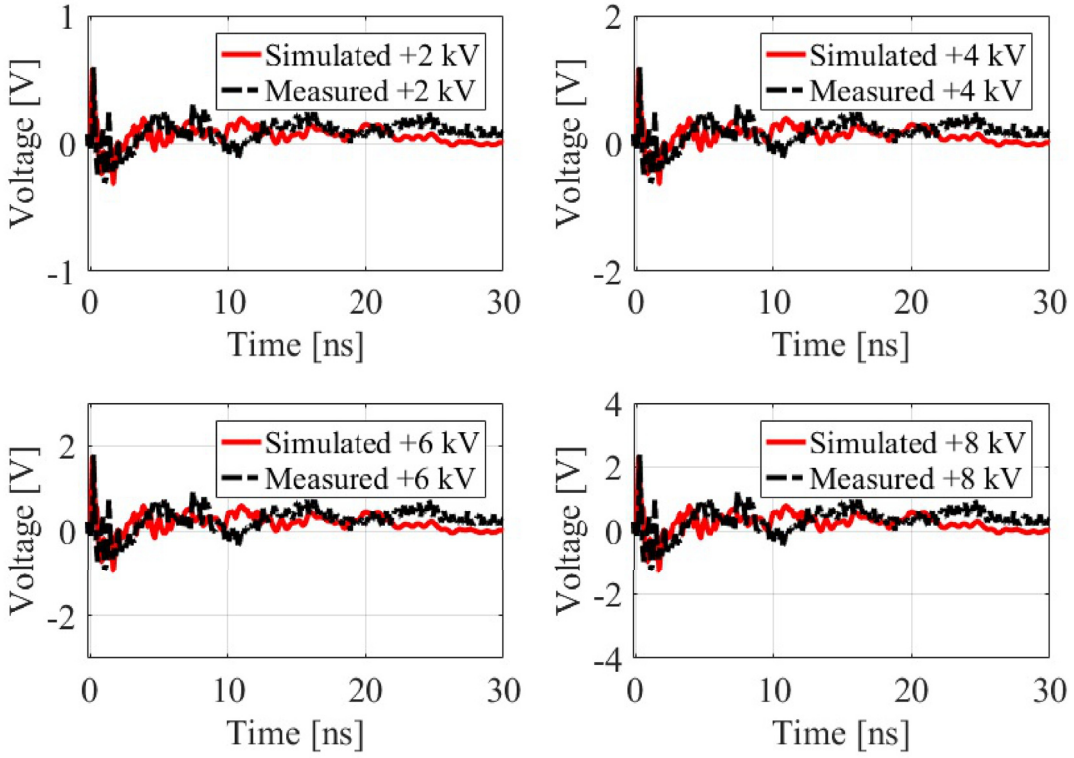

Fig. 7. Comparison of simulated and measured induced ESD voltage for μ-strip line PCB for various ESD discharge voltage levels.

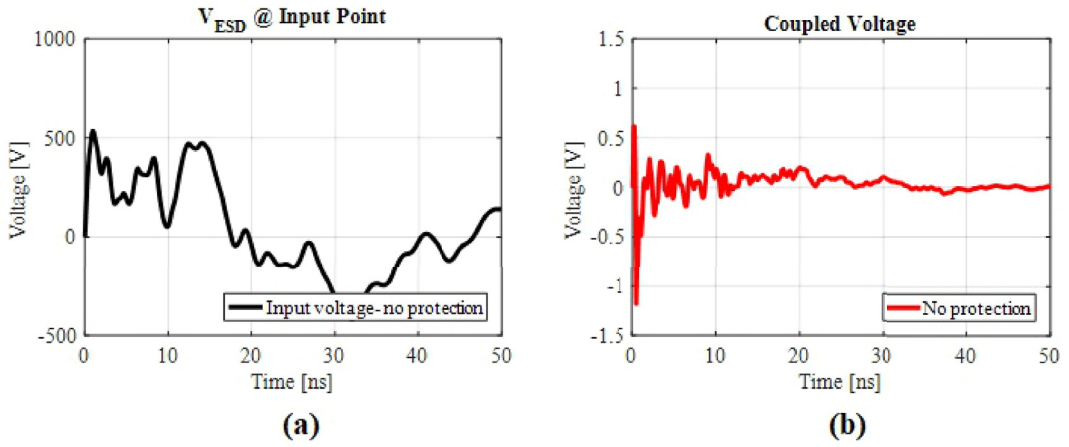

Fig. 8. Micro-strip line PCB results without any protection for +2 kV input voltage level (a) V_{ESD} at input point, (b) $V_{coupled}$ at load point.

3.1. Primary ESD protection

Fig. 9 depicts the schematic for the ESD coupling noise analysis using primary ESD protection scheme. In the primary ESD protection scheme, an ESD protection device (ESD11L5 0DTG transient voltage suppressor (TVS) diode [19]) is installed at the source end to provide the protection to the whole connected system. The SPICE model of the selected diode model is exported in ADS as a component library [19]. After that the diode library model is inserted in circuit schematic as shown in Fig. 9.

The comparison of the coupled noise voltages with and without ESD protection device is shown in Fig. 10. It can be noted from Fig. 10 (a) that the installation of the protection diode at the source point has significantly filtered out the ESD noise at the source point as the maximum V_{ESD} level at the input point is around 1.8 V which is much less than the observed voltage level of around 500 V at the input point in no protection case as illustrated in Fig. 8. Consequently, the induced voltage at load end is almost zero with the installed protection device at the source point as can be noted from Fig. 10 (b) results.

3.2. Secondary ESD protection

The second possible strategy is the placement of the protection device before the load point as illustrated in Fig. 11 which is termed as secondary ESD protection scheme here. This strategy only provides the protection to the load.

The results of induced ESD noise with secondary ESD protection strategy are shown in Fig. 12. It can be noted from Fig. 12 that the observed voltage level at the source point is quite high (similar to no protection case of Fig. 8 (a)). Also the comparison of Fig. 12 (b) wave-

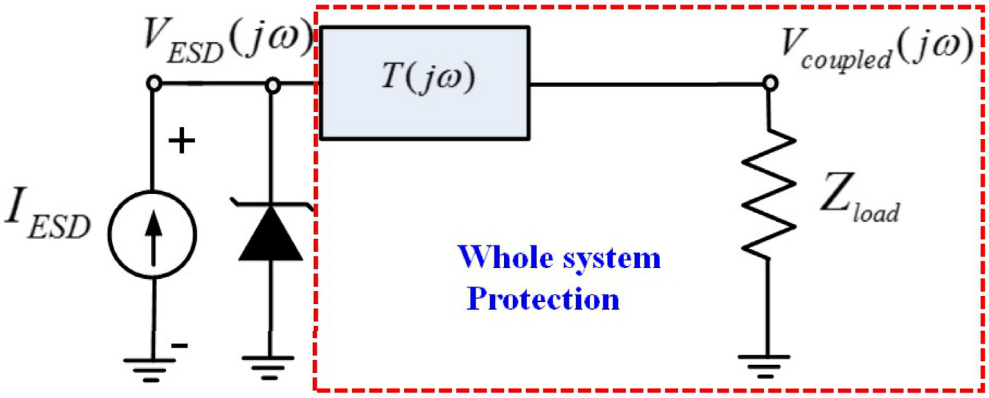

Fig. 9. Induced voltage calculations with primary ESD protection scheme.

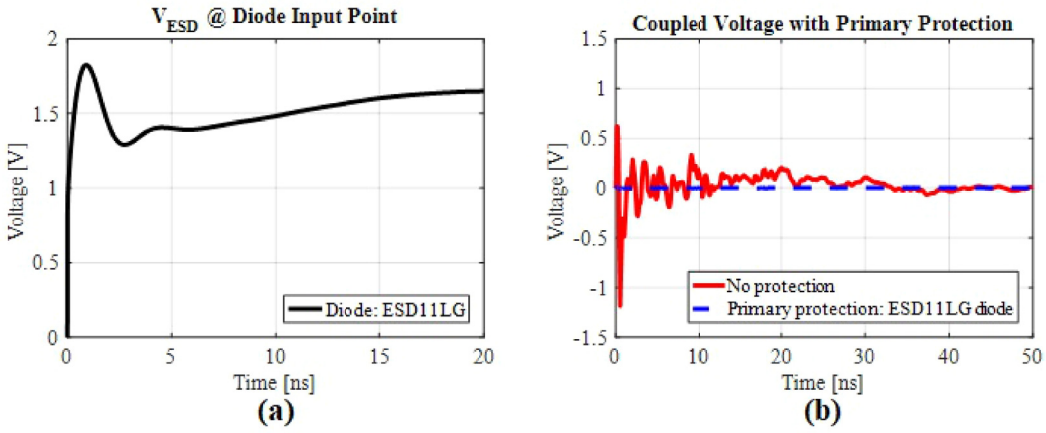

Fig. 10. ESD induced noise voltage results with primary ESD protection scheme for +2 kV input voltage level for μ-strip line PCB (a) V_{ESD} at input point, (b) $V_{coupled}$ at load point.

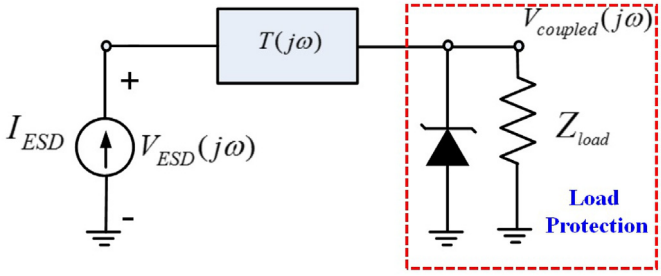

Fig. 11. Induced voltage calculations with secondary ESD protection scheme.

forms with Fig. 8 (b) shows that coupled voltage waveform and level with secondary protection scheme are almost similar to the induced voltage results of no protection scheme. Here, the installed TVS diode at the load end did not trigger due to the low level of input voltage at diode (lower than its threshold voltage) point and consequentially the coupled noise is not filtered out. It shows that installation of the protection diode near the load point is not useful for the analyzed DUT.

3.3. Double ESD protection

The third possible protection device installation strategy is the placement of protection device at both locations *i.e.* after the source point and before the load point. Fig. 13 shows this double protection scheme and it is basically the combination of both primary and secondary protection schemes.

The comparison of the double protection strategy with primary and secondary protection methods is depicted in Fig. 14 (b). It can be observed from Fig. 14 and Table 1 that the coupled voltage levels with double protection are same as with only primary protection strategy of Fig. 9. It deduces that the installation of protection device at the source point is enough to suppress the conduced ESD noise to the load for the analyzed μ-strip line PCB.

3.4. Effect of protection device type on protection strategy

This section presents an analysis of the effect of the different kinds of protection devices on the minimization of the induced coupling. The analysis is performed with four different kinds of diodes as protection devices using primary protection strategy. The selected didoes models for analysis includes three ESD protection diode models: ESD11L50DTG [19], ESD8040 [20] and P6ke200a TVS [21]. Another general transient voltage suppressor (TVS) diode model *i.e* 1v5ke400a TVS [22] is also chosen for the rigorous analysis.

Fig. 15 shows the recorded input voltages at installed diode points (V_{ESD}) and induced voltages ($V_{coupled}$) at the load point for all the analyzed diode types. The comparison of maximum and peak to peak coupled voltage levels for different analyzed cases is depicted in Table 2.

It can be noted from Fig. 15 (a) that the observed voltage levels at the diode points are different for different suppression devices. The highest input voltage levels is observed for the general TVS diode (1v5ke400a TVS). Fig. 15 and Table 2 show the variations of the suppressing input ESD noise for different employed protection devices. The

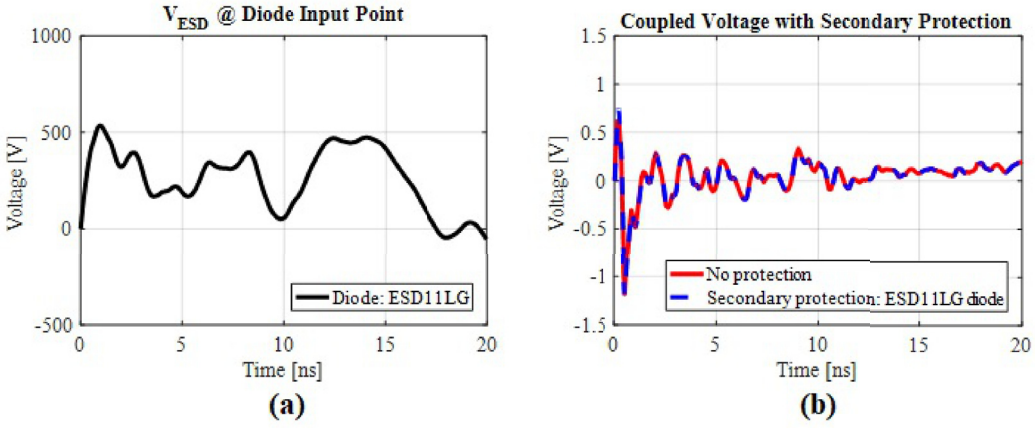

Fig. 12. ESD induced noise voltage results with secondary ESD protection scheme for +2 kV input voltage level for μ-strip line PCB (a) V_{ESD} at input point, (b) $V_{coupled}$ at load point.

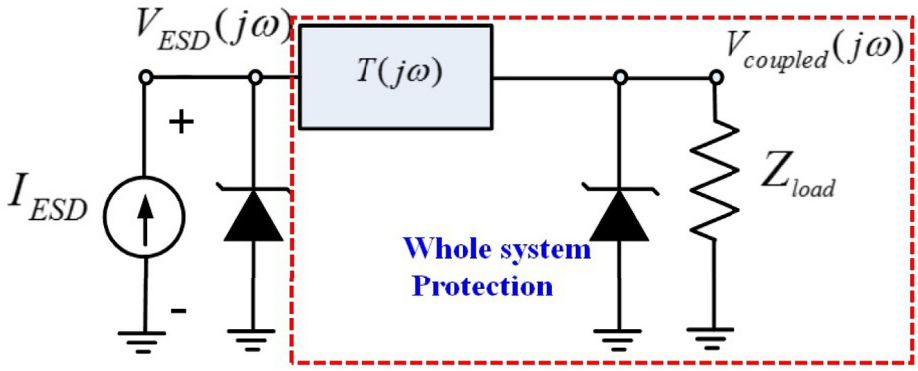

Fig. 13. Induced voltage calculations with double ESD protection scheme.

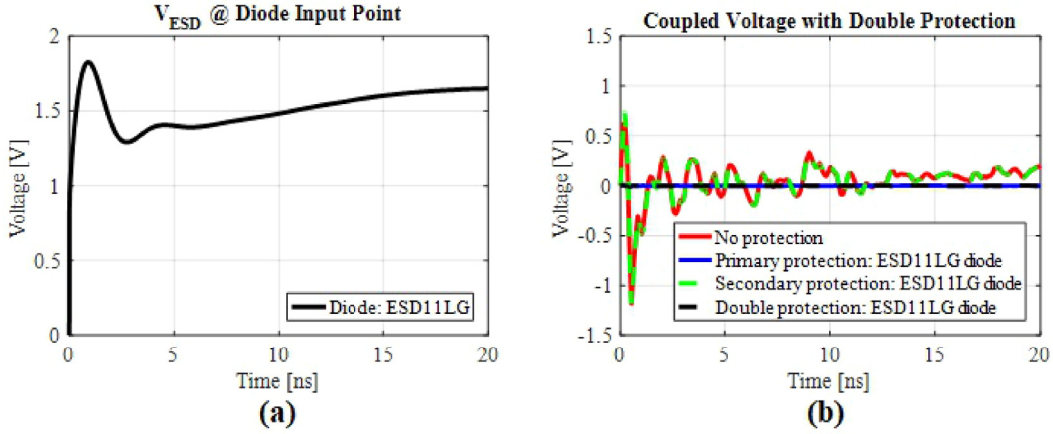

Fig. 14. ESD induced noise voltage results with double ESD protection scheme for +2 kV input voltage level for μ-strip line PCB (a) V_{ESD} at input point, (b) $V_{coupled}$ at load point.

Table 1
Comparison of coupled ESD noise voltage at load for different ESD protection strategies (waveform results in Fig. 14) (b) for μ-strip line PCB.

	No protection		Primary protection		Secondary protection		Double protection	
DUT	Max [V]	PP [V]	Max [V]	PP [V]	Max [V]	PP [V]	Max [V]	PP [V]
μ-strip PCB	0.62	1.8	0.005	0.015	0.75	1.95	0.005	0.015

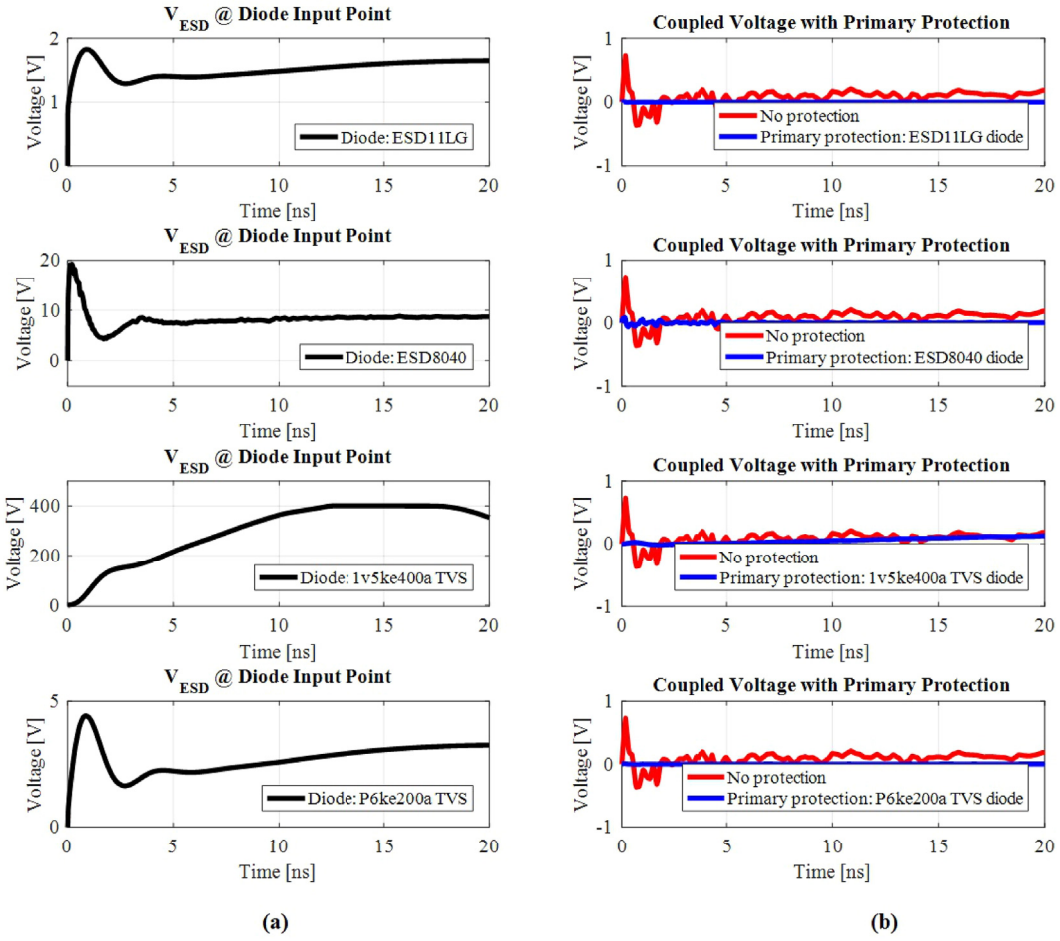

Fig. 15. Input and coupled ESD voltages with different kinds of ESD suppression devices for +2 kV input voltage level (a) V_{ESD} at input point for each diode, (b) $V_{coupled}$ at load point for each diode.

Table 2
Comparison of coupled ESD noise voltage at load for different ESD suppression devices (waveform results in Figs. 15 and 16) for μ-strip PCB.

		Max [V]	PP [V]
Diodes	No Protection	0.62	1.8
	ESD11LG	0.005	0.015
	ESD8040	0.09	0.26
	1v5ke400a TVS	0.12	0.20
	P6ke200a TVS	0.009	0.023
Snapback devices	SCR (es103d)	0.008	0.017
	SCR (s402es)	0.011	0.004
	GGNMOS	0.62	1.8
	GCNMOS	0.34	0.95

results shows that ESD11L5 0DTG and P6ke200a almost completely suppressed the coupled ESD noise. The general TVS diode '1v5ke400a', although had minimized the coupling noise maximum levels to 0.12 V from 0.62 V, its protection characteristics are ranked lowers in the analyzed group of four diodes.

The impact of the snapback ESD suppression devices is also analyzed. Two different models of silicon controlled rectifier (SCR) (es103d and s402es [23]), grounded-gate N-type metal-oxide-semiconductor (GGNMOS) and gate-coupled NMOS (GCNMOS) transistors are used for the case study analysis. The snapback effect in such devices occurs due to the bipolar junction transistor parasitic and they are triggered by the variations in the substrate current [3,5]. The spice models of SCR devices are obtained from Ref. [23]. The GGNMOS and GCNMOS are modeled in ADS using simple NMOS based on IBM 0.13 µm CMOS technology. The chosen length and width of NMOS are 0.18 µm and 300 µm respectively for the analyzed cases. The gate-coupled resistor for the used GCNMOS is 10 kΩ.

Fig. 16 depicts the results for the analyzed snapback devices for the microstrip line PCB DUT. It can be observed from the results of Fig. 16 and Table 2 that the SCR devices have almost completely suppressed the coupling ESD noise. The GCNMOS performed better than GGNMOS for the analyzed case. The GGNMOS did not suppress the coupling ESD noise for the testing device which could be due to the used simple NMOS for the analysis purpose. The proper design of the NMOS could results in better results in terms of minimization of the coupling ESD noise [3,5].

3.5. Analysis of ESD protection for various ESD stressing levels

The effect of the changing ESD stressing levels on the chosen ESD protection scheme with selected protection device can be analyzed quickly by just changing the input ESD current waveform (I_{ESD}) in the circuit simulator. The ESD current waveforms corresponding to the various ESD levels *e.g.* +2 kV, +4 kV, +6 kV and +8 kV, can be obtained quickly from the circuit model (see Fig. 3) of the ESD generator.

The effect of the change in zapping levels is analyzed with primary protection scheme and P6ke200a diode as protection device for the μ-strip line PCB. Fig. 17 illustrate the variations in the V_{ESD} and $V_{coupled}$ for the +2 kV, +4 kV, +6 kV and +8 kV ESD zapping levels with no

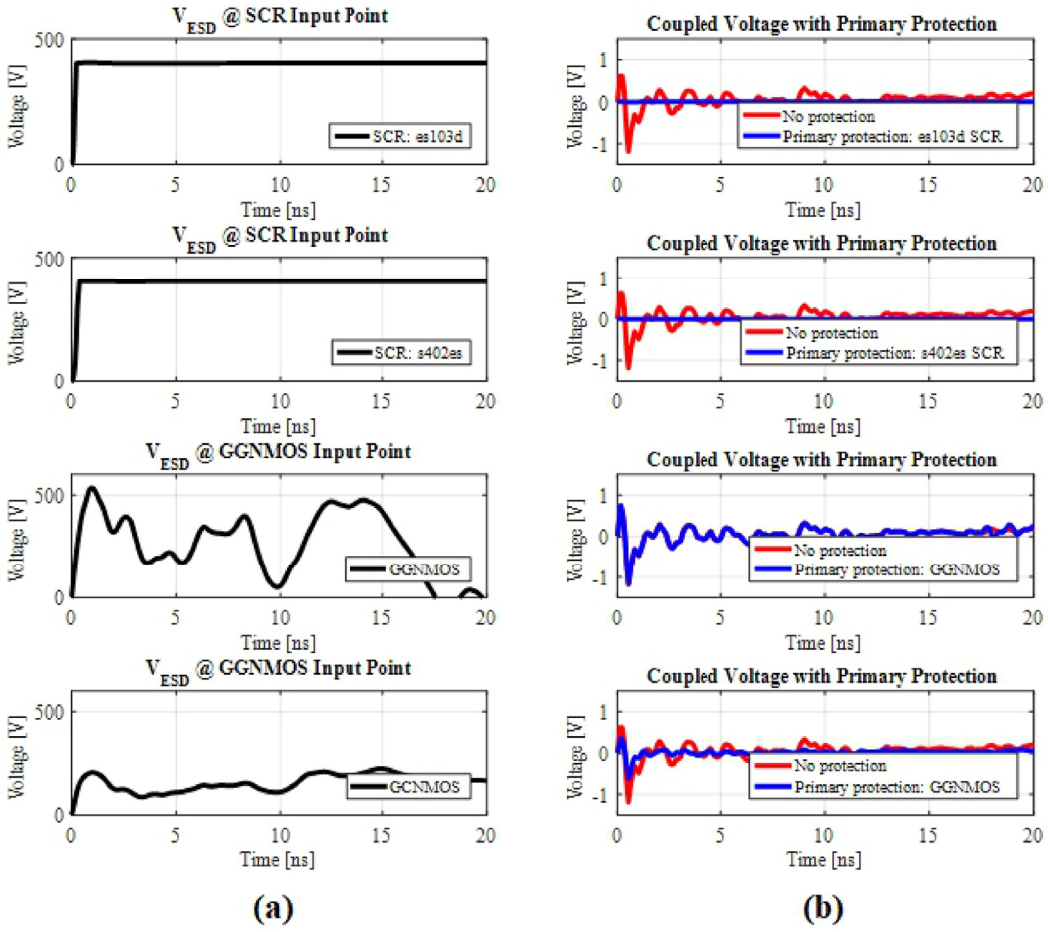

Fig. 16. Input and coupled ESD voltages with different kinds of snapback suppression devices for +2 kV input voltage level (a) V_{ESD} at input point for each device, (b) $V_{coupled}$ at load point for each device.

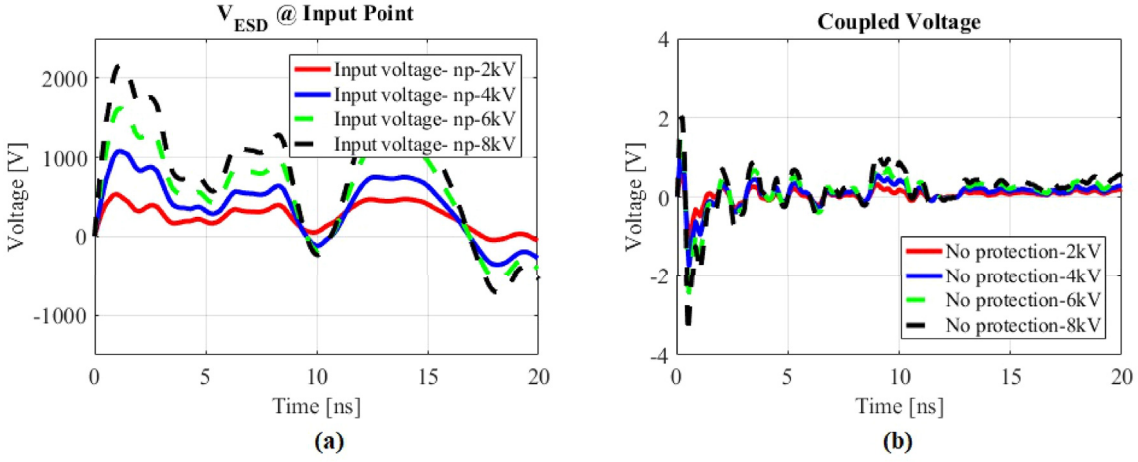

Fig. 17. Input and coupled ESD voltages with changing ESD stressing levels for μ-strip line PCB with no protection (a) V_{ESD} at input point, (b) $V_{coupled}$ at load point.

employed protection. The waveforms show that both V_{ESD} and $V_{coupled}$ levels increases with the gradual enhancement of the ESD stressing levels.

The change in the input and coupled voltage levels with the insertion of the ESD suppressing P6ke200a diode at primary side is depicted in Fig. 18. The level of the coupled voltages for the various ESD zapping levels in Fig. 18 (b) reflects that the used ESD protection device is successful suppressing the coupling ESD noises for the analyzed ESD zapping levels.

The developed analysis strategy could provide ease to the ESD/EMC design engineers to quickly estimate the impact of the change in the ESD stressing levels on the coupling noise minimization capabilities of the chosen ESD protection device.

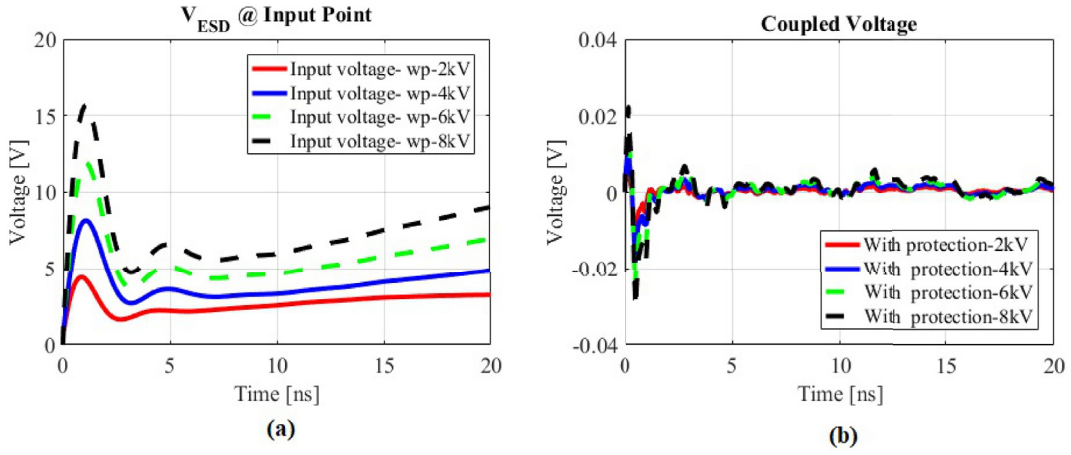

Fig. 18. ESD induced noise voltage results with primary ESD protection scheme for various ESD stressing levels for μ-strip line PCB (a) V_{ESD} at input point, (b) $V_{coupled}$ at load point.

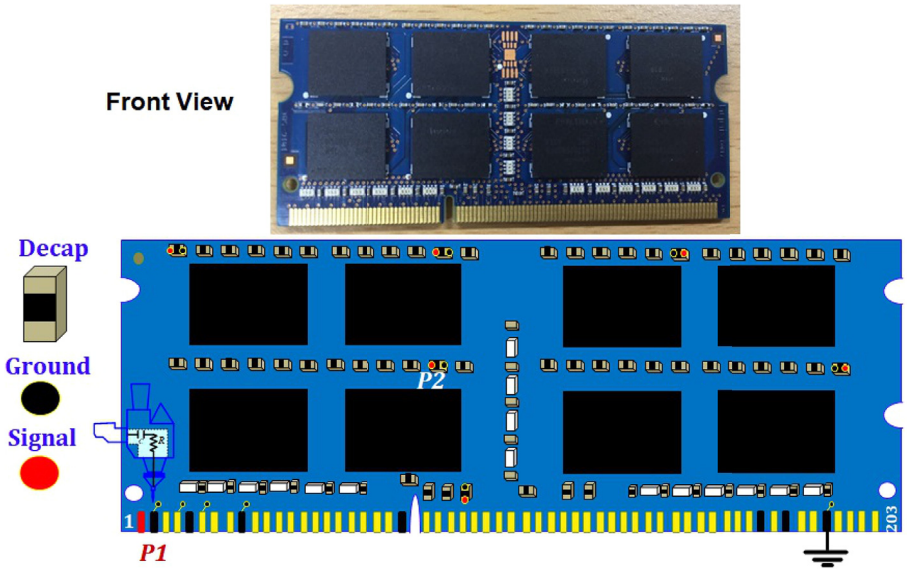

Fig. 19. Schematic of 4 GB DRAM memory module.

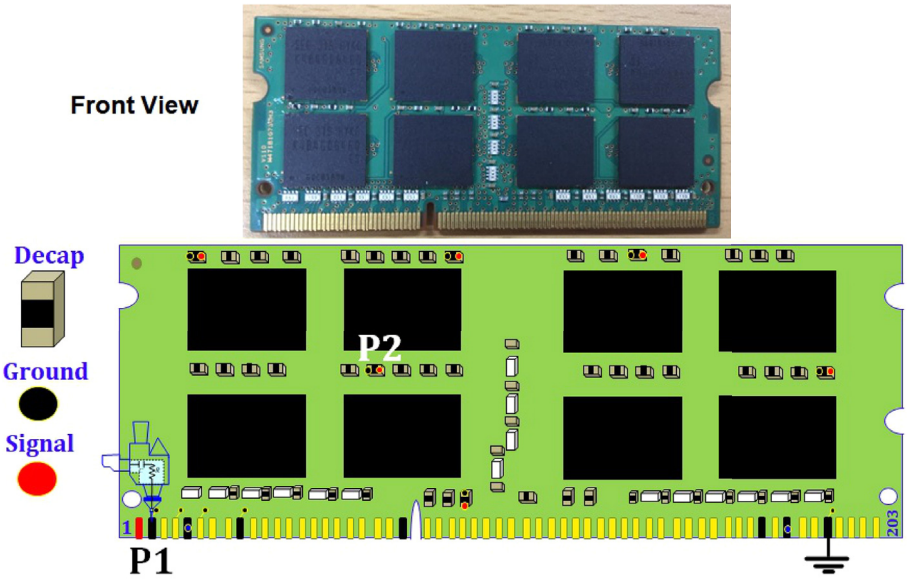

Fig. 20. Schematic of 8 GB DRAM memory module.

4. Design of ESD protection scheme for mobile device memory modules

The second case study analysis is about the analysis of ESD protection for high-speed small outline dual in-line memory module (SO-DIMM) DRAM modules of a smart device. The analysis is performed for the real commercial high-speed 4 GB and 8 GB DRAM memory modules.

Figs. 19 and 20 depict the schematics of the 4 GB and 8 GB DRAM memory modules respectively. Each memory modules constitutes of 8 SODIMM chips on the front and backsides. In Figs. 19 and 20, 'P1′ is the ground plane of memory module and it represents the zapping point of ESD gun. The victim point 'P2' is defined across a decap for both memory modules as illustrated in Figs. 19 and 20 respectively.

The two-port *S*-parameters are measured between the points 'P1′ and 'P2′ for each memory module using the measurement setup of Fig. 21. The coaxial cables are connected between points 'P1′ and 'P2' for the *S*-parameter measurements (see Ref. [18] for details about the measurement procedure). The measured *S*-parameter are converted to the coupling transfer impedance function for the induced ESD coupling analysis and rapid design of ESD protection using the proposed method.

Figs. 22 and 23 show the induced noise voltages at 'P2′ with and without ESD protection for 4 GB and 8 GB DRAM memory modules respectively. The coupled voltage waveform for 4 GB DRAM module in Fig. 22 (a) illustrates that the maximum induced noise voltage level is around 6.5 V for the +2 kV ESD discharge level without any protection. By using the P6ke200a diode as primary ESD protection, it can be noted from Fig. 22 (b) that the maximum coupled noise voltage level has been reduced to the value of 0.05 V. Similar results can be observed for the 8 GB DRAM memory module in Fig. 23. The insertion of P6ke200a diode as primary ESD protection device completely suppress the cou-

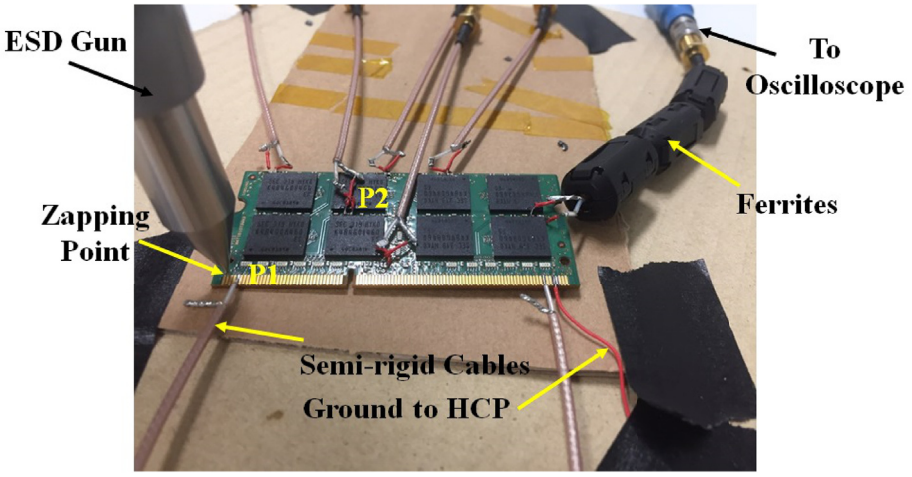

Fig. 21. Frequency domain measurement setup for the 8 GB DRAM memory module.

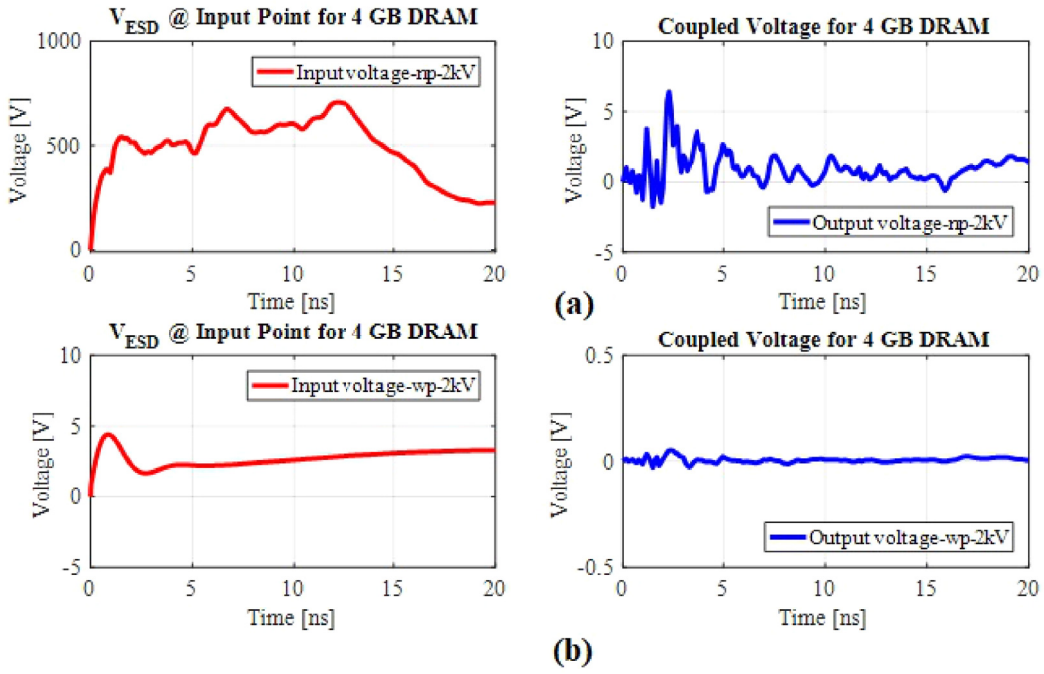

Fig. 22. ESD induced noise voltage results with primary ESD protection scheme for +2 kV input voltage level for 4 GB DRAM memory module (a) V_{ESD} at input point, (b) $V_{coupled}$ at load point.

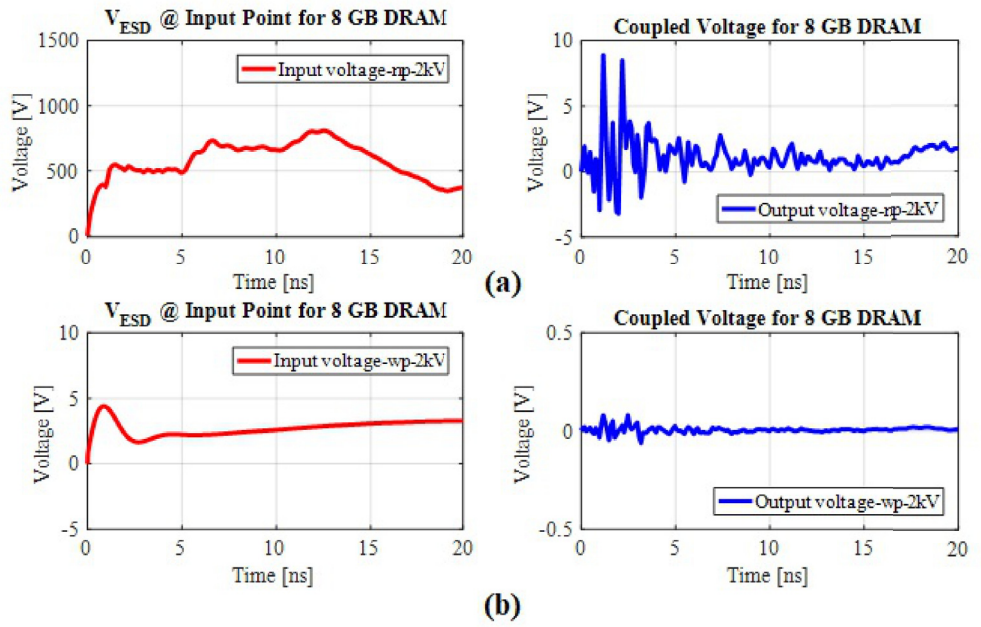

Fig. 23. ESD induced noise voltage results with primary ESD protection scheme for +2 kV input voltage level for 8 GB DRAM memory module (a) V_{ESD} at input point, (b) $V_{coupled}$ at load point.

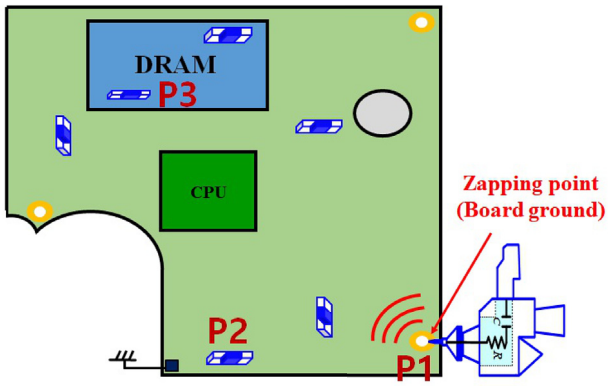

Fig. 24. Schematic of commercial laptop motherboard.

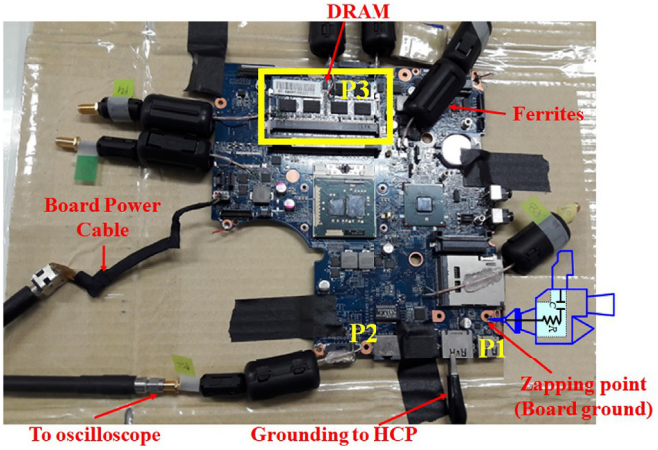

Fig. 25. Frequency domain measurement setup for the laptop motherboard.

pling ESD noise levels across the decap installed at the 'P2' location of memory module. The maximum value of coupled ESD noise has been reduced to 0.08 V with primary ESD protection from the 8.88 V value of no protection case for 8 GB DRAM memory module.

5. Design of ESD protection scheme for laptop motherboard

For the demonstration of the effectiveness of the proposed procedure of rapid ESD protection design for real time DUTs, the third case study analysis was performed with a working motherboard of commercial notebook.

The schematic of the analyzed laptop motherboard is shown in Fig. 24. Here, two victim points ('P2′ and 'P3′) are selected on the actual motherboard as illustrated in Fig. 24. The chosen 'P2′ decap is near the zapping point (P1) while the second victim point 'P3' is away from the zapping point. Frequency domain characterization setup for the *S*-parameter measurements of each pair *i.e.* 'P1–P2′ and 'P1–P3' of operating motherboard is shown in Fig. 25. The details about the measurement procedure can be found in Ref. [17].

Fig. 26 depicts the V_{ESD} at input side and coupled ESD noise voltages for 'P2′ point with and without employed ESD protection. The results of Fig. 26 (a) reflects that higher level of ESD noise (maximum value of 11 V) is transferred from the zapping point (P1) to the victim location of 'P2′ when +2 kV ESD waveform is zapped at the ground plane of the motherboard *i.e.* 'P1' point. The installation of the P6ke200a diode across the signal and ground plane (primary ESD protection) of the motherboard reduces the maximum value of the noise levels to 0.08 V as shown in the couple noise waveform of Fig. 26 (b).

The coupled noise voltage results of Fig. 27 (a) shows that the coupled ESD noise is lower for the 'P3′ point as it is comparatively far-away from the aggressor point (P1) as compared to the 'P2' location. The suppression of the coupled ESD noise can be noted in Fig. 27 (b) after the installation of the design ESD protection scheme.

6. Conclusion

In this work, a new fast and efficient approach for the assessment and designing of the system level ESD protections strategy for high-speed microelectronic devices based on the coupling transfer

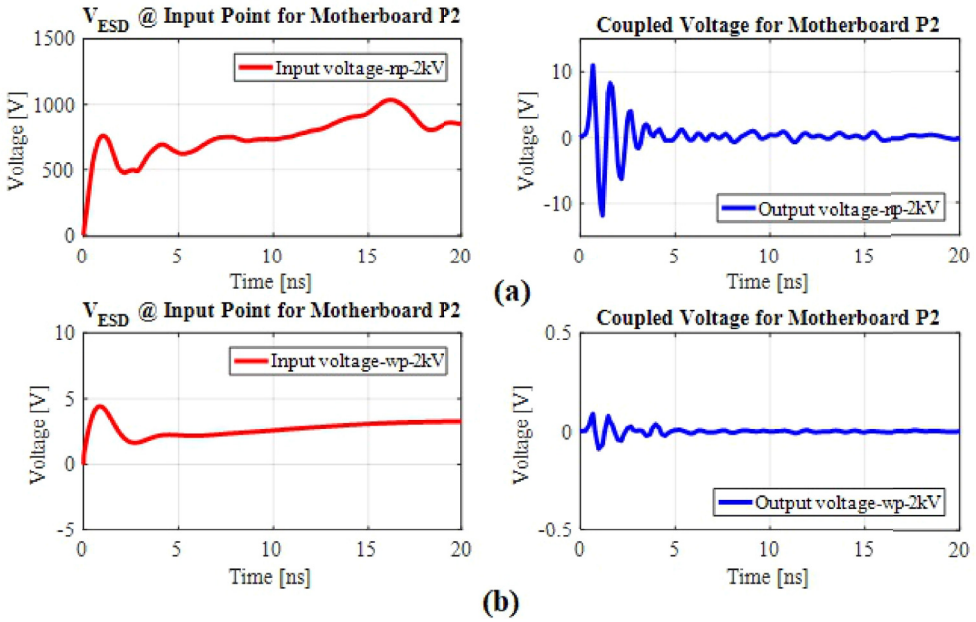

Fig. 26. ESD induced noise voltage results with primary ESD protection scheme for +2 kV input voltage level for laptop motherboard at P2 (a) V_{ESD} at input point, (b) $V_{coupled}$ at load point.

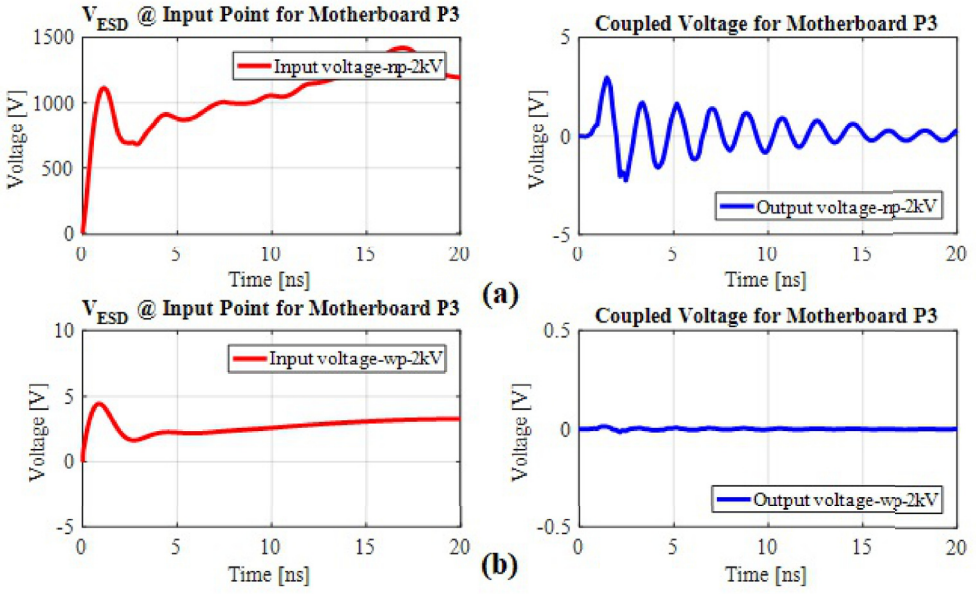

Fig. 27. ESD induced noise voltage results with primary ESD protection scheme for +2 kV input voltage level for laptop motherboard at P3 (a) V_{ESD} at input point, (b) $V_{coupled}$ at load point.

impedance function is discussed. After the validation of the designed circuit simulator based analysis setup, the study explained the role of primary, secondary and, double ESD protection schemes along with various kinds of protection devices on the coupling ESD noises for a prototype microstrip line PCB. Subsequently, the efficient ESD protection schemes for commercial high-speed DRAM memory modules of a smart device and an operating motherboard of a mobile notebook are designed. The suggested procedure for the designing of the ESD protection strategy and analysis of the various suppression devices confirms that the proposed procedure could be useful for the EMI/EMC, ESD and qualification engineers for the fast identification of the best ESD protection device by quickly analyzing the coupling noise levels in circuit simulator for the various input ESD stressing levels.

Author statement

Jawad Yousaf, Wansoo Nah: Conceptualization, Methodology, Software. Jawad Yousaf, Eqab Rateb Al Majali, Hassan Saif: Data curation, Writing- Original draft preparation. Jawad Yousaf, Hassan Saif, Hatem Rmili: Visualization, Investigation. Wansoo Nah: Supervision.: Jawad Yousaf, Hassan Saif, Eqab Rateb Al Majali,: Software, Validation. Jawad Yousaf, Wansoo Nah, Hassan Saif: Writing- Reviewing and Editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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