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A Scalable and Integrated Reconfigurable Intelligent Surface

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ABSTRACT

A scalable reconfigurable intelligent surface (RIS) architecture with both centralized and distributed control capability is presented. The RIS is implemented using a one-bit phase reconfigurable unit cell (UC) designed for X-band operation. The UC is realized by embedding a PIN diode into a slotted copper patch, achieving a maximum phase shift at 9.5 GHz with a phase difference of 180° ± 20° across the 9–10 GHz band. The proposed RIS enables real-time reconfiguration, with each element controlled through an FPGA achieving an update time below 0.1 ms. In addition, multiple control interfaces are supported, including LAN, USB, and WiFi. The measurement results of a 16 × 16 single RIS tile prototype validate beam steering from −50° to 50° and gain performance, demonstrating a peak gain of 20.2 dBi at broadside $\theta = 0°$ and 18.2 dBi at $\theta = \pm 50°$. To demonstrate scalability, a four-tile prototype of 32 × 32 (each tile consisting of 16 × 16 UCs) is fabricated. Each tile can be independently programmed via its dedicated interface, or alternatively, a single interface module (WiFi, LAN, or USB) can distribute ON/OFF configurations across all tiles, thereby enabling flexible and scalable control of the RIS.

1 | Introduction

In the current technological era, wireless communication systems are experiencing rapid transformation driven by unprecedented data growth, widespread adoption of mobile devices, and cloud-based Internet of Things (IoT) applications [1, 2]. These increasing demands push existing wireless infrastructures to their limits, highlighting the need for novel approaches capable of efficiently controlling electromagnetic (EM) propagation and enhancing spectrum utilization. Metasurfaces have attracted significant attention in the past decade as a promising approach to control EM waves through subwavelength engineered structures [3–5], which can be exploited to manipulate EM waves for polarization conversion [6], generating multiple beams [7], orbital angular momentum (OAM) beams in the far-field [8, 9], as well as multiple foci and nulls in the near-field [10]. However, conventional passive metasurfaces are inherently static, offering fixed functionality once fabricated and lacking the ability to dynamically adapt to changing wireless environments. However, conventional passive metasurfaces are inherently static, offering fixed functionality once fabricated and lacking the ability to dynamically adapt to changing wireless environments. This limitation restricts their use in modern communication systems that demand reconfigurability and real-time beam control. To overcome this challenge, intelligent and reconfigurable RF front-end devices have been proposed as key enablers for next-generation wireless infrastructures, allowing enhanced functionality and efficient utilization of limited spectral and hardware resources. In this context, RIS has attracted significant research attention because it provides the ability to flexibly control the electromagnetic response of the system without physically altering its geometry [11, 12]. This feature is especially desirable in scenarios that demand

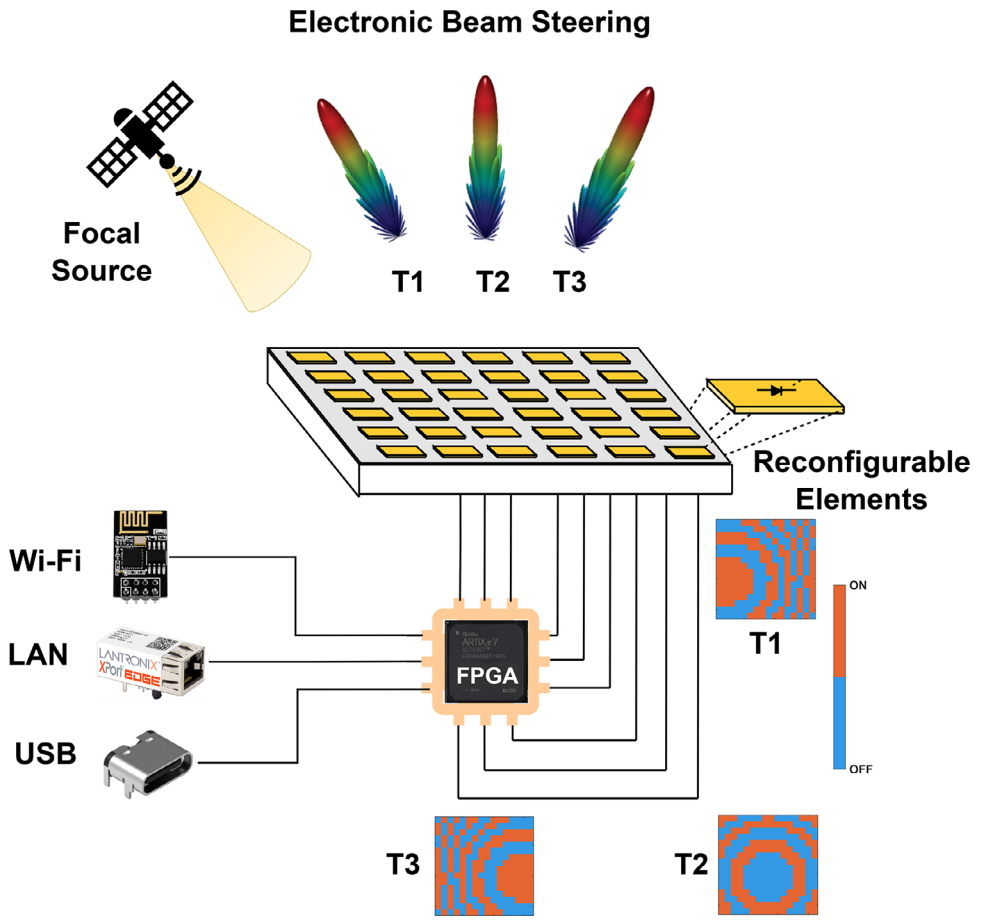


FIGURE 1 | Conceptual diagram of a single RIS tile with integrated FPGA and multi-interface control (UART, Wi-Fi, LAN).

multi-functionality, frequency agility, and adaptive beamforming, all of which are central to modern wireless networks.

Various implementation techniques have been developed to realize reconfigurability in RF components. These include micro-electromechanical systems (MEMS) [13], PIN diodes [14–16], varactor diodes [17–19], and photo-conductive switches [20], as well as tunable materials such as ferrites [21], liquid crystals [22], and phase-change or resistive materials such as vanadium dioxide (VO_2) [23]. Each of these technologies enables manipulation of fundamental RIS parameters such as resonant frequency, bandwidth, polarization, beam direction, and radiation efficiency. For instance, PIN diodes provide fast electronic tuning capabilities, while liquid crystals, VO_2, and varactors allow continuous tuning of EM properties. Although RIS with continuous phase tunability offer fine-grained control and superior beamforming flexibility, they typically suffer from higher insertion losses, increased biasing complexity, and limited scalability, particularly at higher frequencies, which restrict their suitability for compact, low-power, and cost-sensitive applications.

Simplified RIS designs have therefore emerged in recent years, often based on electronically controlled single-pole–single-throw (SPST) switches—most commonly implemented using RF MEMS or PIN diodes. These switches provide discrete control over reflection or transmission states, enabling straightforward and reliable phase or amplitude reconfiguration. Among the possible quantization schemes, one-bit phase quantization has been widely investigated due to its simplicity and ease of integration in large-scale arrays [24–26]. In this scheme, each UC can switch between two discrete phase states separated by 180°, enabling basic beam steering and pattern shaping. The one-bit phase quantization introduces only a minor performance penalty, with about 3, 2.8, and 2.4 dB gain reductions compared with continuous-phase, three-bit, and two-bit configurations, respectively, while preserving similar beamwidth and steering accuracy [27], which, together with its low cost, reduced control complexity, and scalability, makes it highly attractive for practical reflectarray or metasurface implementations.

Nevertheless, one-bit quantization inherently introduces phase discretization errors that degrade array performance by reducing beamforming accuracy, gain, and sidelobe suppression. Although these limitations are well documented, the trade-off between performance and simplicity often favors one-bit designs in many wireless communication applications [14, 28, 29]. For IoT and mobile communication scenarios, performance penalties are generally acceptable when weighed against substantial hardware efficiency and system-level practicality, making one-bit RIS designs a compelling low-cost and energy-efficient solution [14].

Most existing RIS designs rely on external control circuits implemented using platforms such as FPGA, Arduino, or Raspberry Pi. While these approaches offer flexibility, they often suffer from limited update speed and poor scalability. In many cases, control data is transferred serially via shift registers, constraining

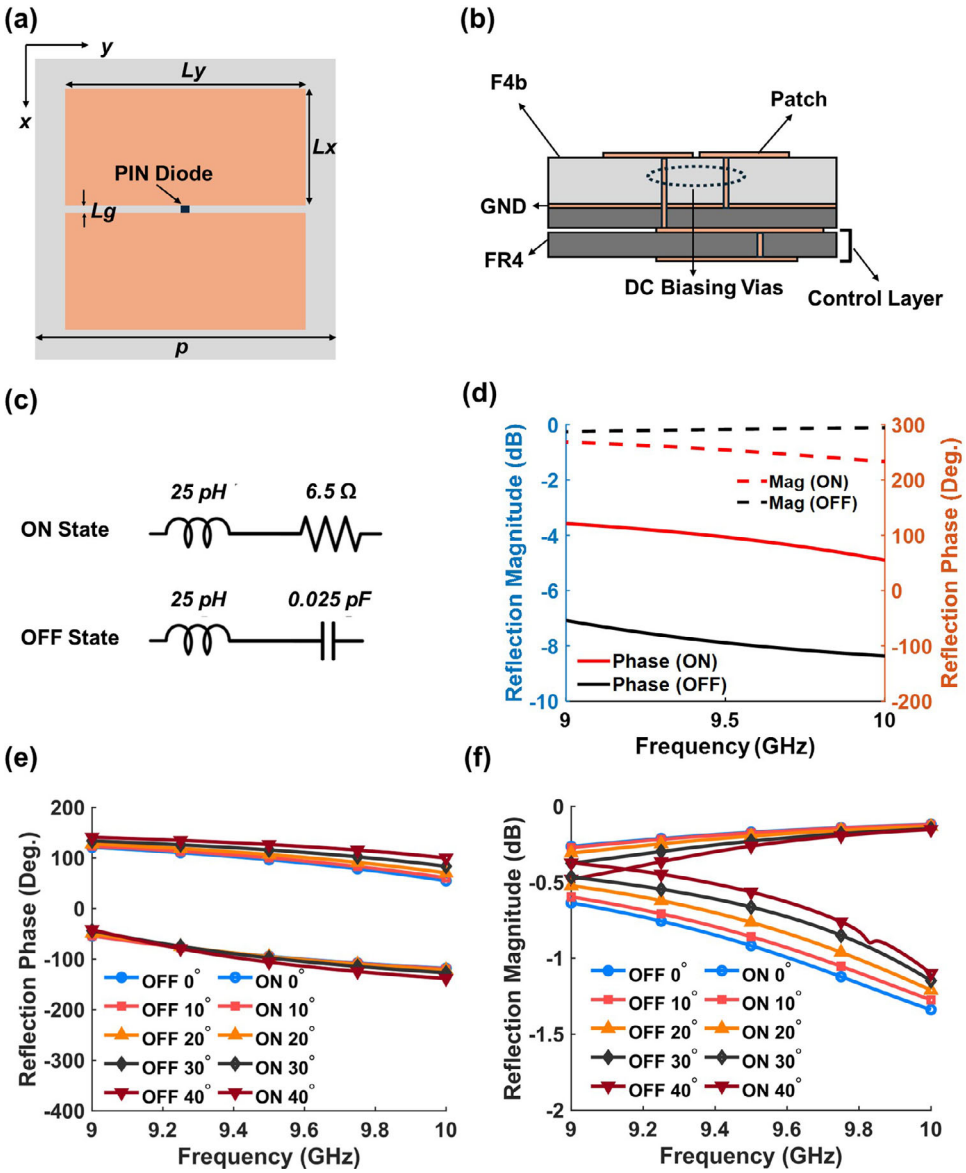


FIGURE 2 | one-bit phase reconfigurable RIS element, (a) Front view, (b) Side view, (c) Diode's equivalent RLC circuit, (d) Simulated reflection magnitude and phase, (e) Reflection phase with incident angles up to 40°, (f) Reflection magnitude with incident angles up to 40°.

reconfiguration speed. Parallel FPGA connections improve speed but remain practical only for small-scale RIS due to wiring complexity. Furthermore, external control modules connected by cables add bulk and complicate integration. As a result, even when the RF portion of an RIS is scalable, the control infrastructure often becomes the bottleneck.

To overcome these challenges, we propose a novel one-bit RIS architecture that integrates the entire control system directly onto a single four-layer printed circuit board (PCB). An FPGA chip is embedded within the PCB, eliminating the need for external wiring or hardwired connections to control the individual elements. This fully integrated design reduces physical complexity while enabling versatile, high-speed control. In addition, the RIS can be accessed and managed through multiple interfaces, including UART, Wi-Fi, and LAN, offering flexible operation suitable for real-time and scalable wireless applications. The proposed architecture is inherently scalable: a single tile, consisting of 16×16 unit cells, is shown in Figure 1, which can operate independently, while multiple tiles can be cascaded to form larger RIS panels. In our prototype, four tiles were combined to realize a 32×32 RIS, where each tile can be addressed individually through its integrated control interface. Additionally, RIS can be collectively controlled through a single interface device, such as Wi-Fi, USB, or LAN, thereby demonstrating both centralized and distributed control capabilities for large-scale deployments.

2 | RIS Design

2.1 | Design Analysis of Unit Cell

In this section, the structure of the one-bit RIS UC along with reflection characteristics are discussed. As shown in Figures 2a,b, the UC consists of three metallic layers etched on two dielectric substrates. The metallic layer on the top has a square patch with a

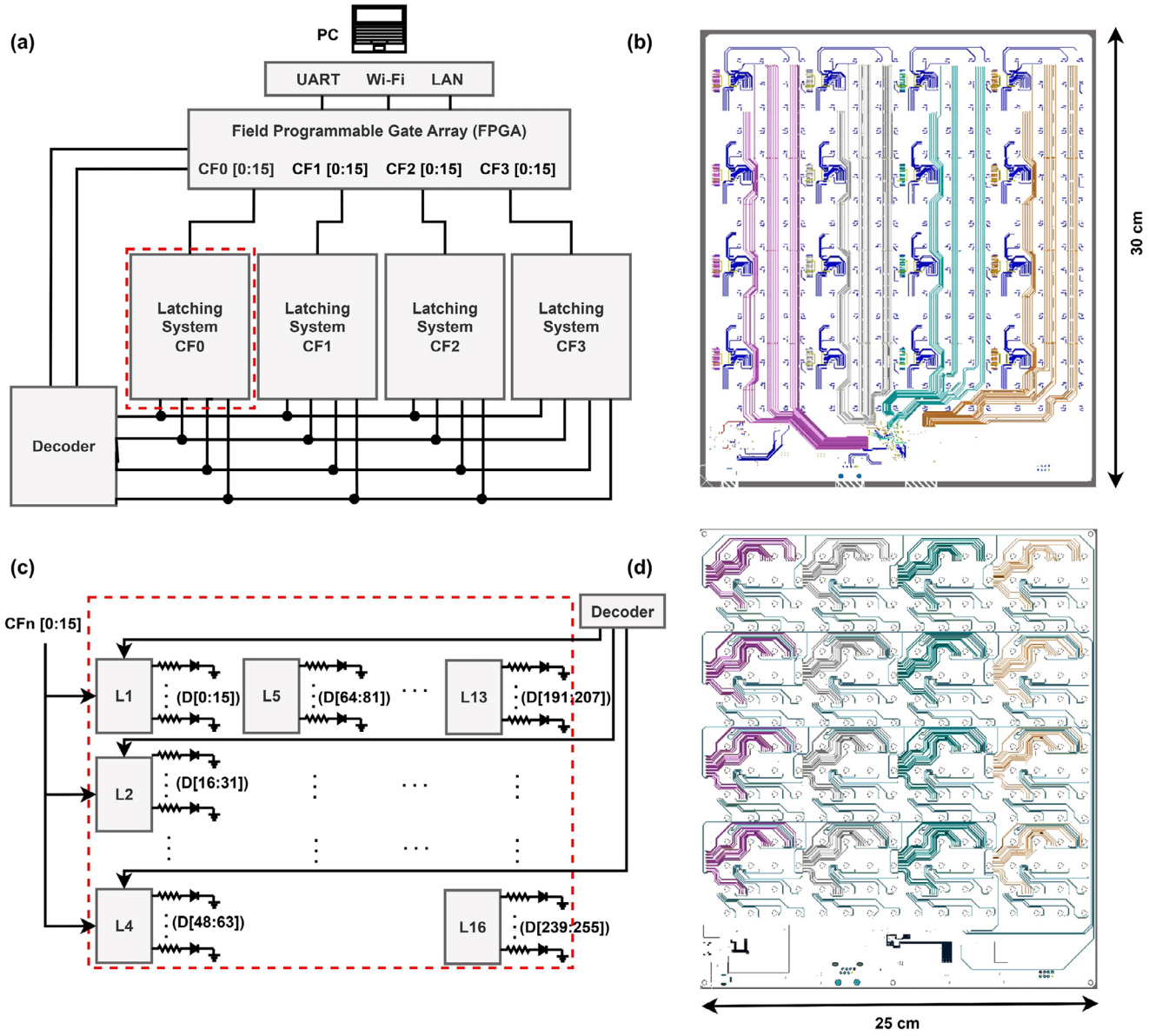


FIGURE 3 | Integrated control architecture of a single 16 × 16 RIS tile: (a) FPGA output ports and latching subsystems, (b) PCB routing layout with color-coded CF subsystems, (c) latch and decoder operation for selective diode control, and (d) actual PCB layout showing horizontal control lines to the diodes.

rectangular slot etched on a 1.58-mm-thick F4B substrate having a relative permittivity of 2.65. To add reconfigurability, a PIN diode is used in the slot which enable us to achieve 180° phase shift between two states of diodes. The middle layer acts as a ground plane for both the direct-current (DC) and the radio-frequency (RF). The slot configuration allows two separated patches which control the diode anode and cathode terminals, allowing the DC to complete the loop. The biasing layers are implemented on the two back layers of the ground layer. Fr4 substrate with a thickness of 1mm is used for each biasing layer. To have minimal effect on the UC working principle and eliminate RF loss, the zero-electric-field point on the non-radiating edge of the patch is selected for biasing, as this region carries negligible RF power and thus minimally perturbs the radiating element. To further choke the RF to the biasing circuitry, an open-ended, wideband radial stub is introduced along with a quarter-wavelength microstrip line. The geometrical parameters of the UC are as follows: $L_y = 14$ mm, $L_x = 6.8$ mm, and $L_g = 0.4$ mm. The chosen unit-cell periodicity of $p = 16$ mm ($p/\lambda \approx 0.48$–0.53 over 9–10 GHz) supports beam steering up to ±50° without visible-region grating lobes, linking the unit cell-level stability to the array-level performance.

The switching functionality is implemented using the MADP-000907-14020 PIN diode (MACOM, Lowell, MA, USA), which provides the required phase shift between the two states. It is worth noting here that the PIN diode is modeled with lumped RLC boundary condition in the simulations. Diode equivalent circuits, which are calculated using the s2p data shared by manufacturer, are shown in Figure 1c for the ON and OFF states of the diode. For ON and OFF state, the PIN diode is modeled as a series of lumped resistance (R) and inductance (L), and capacitance (C) and inductance (L), respectively. The

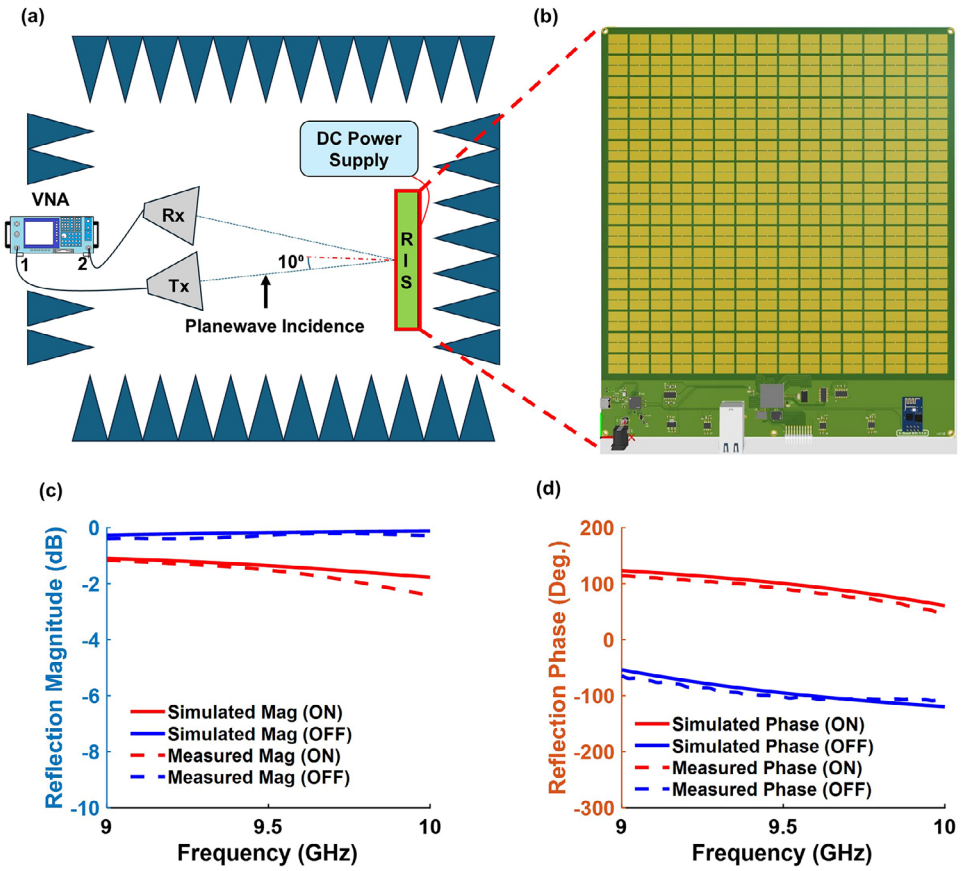


FIGURE 4 | RIS reflection characterization (a) Measurement setup with transmitter and receiver antennas, (b) Simulated versus measured reflection magnitude, (c) Simulated versus measured reflection phase.

UC is modeled and simulated under infinite boundary condition combined with Floquet port excitation in Ansys HFSS 23.0.

The simulated reflection characteristics are plotted in Figure 1d. The dashed and solid lines in the plot represent the magnitude and phase response of UC in diode ON and OFF states, respectively. It can be observed that at 9.5 GHz, the phase difference between the two states of the element are 200° while at the edges of the band (9 – 10 GHz), the phase difference converges to 180°. It indicates a good UC bandwidth performance of 1 GHz in the X-band. The UC reflection loss in the diode OFF-state is less than 0.2 dB across the frequency band of interest. In the ON-state, the loss increases because of the diode series resistance of 6.5 Ω. In any case, the reflection loss remains under 2 dB throughout the band. These results confirm that the element provides low loss one-bit phase reconfigurability, thereby making it a suitable candidate for large-scale RIS implementations. The UC periodicity is $0.52\lambda_0$, where λ_0 denotes the wavelength in free space.

In addition, the UC response for oblique incidence angles are also observed. The oblique-incidence analysis is important because, in practice, the RIS surface is illuminated by a near-field feed, leading to varying incidence angles across the aperture. In the proposed setup, an offset feed with a 15° tilt and F/D ≈ 0.9 produces a maximum incidence angle of about 40°. The reflection amplitude and phase of the unit-cell is shown in Figure 1e,f, respectively with varying incident angles up to 40°. The magnitude response at oblique incidence remains consistent with slightly lower reflection loss at higher angles. Also the phase difference between the ON and OFF states for oblique incidence remained closer to 180°. The phase difference between the two diode states is within the acceptable 180°±20° region for one-bit RIS performance up to an oblique incident angle of ±40°.

2.2 | Control Circuit Design and Prototyping

The proposed RIS prototype was designed using multilayer PCB technology with the layer order shown in Figure 2b. Each tile contains 256 PIN diodes patterned on a 1.6 mm thick F4B substrate using standard photolithography and copper etching processes. The biasing network was etched on the rear side of the board with carefully designed bias lines to minimize electromagnetic interference. PIN diodes were soldered as surface-mount components, and header pins were employed to allow cascading and extension of the power supply and configuration update to more RIS tiles.

The proposed control architecture allows the FPGA to manage all 256 diodes using 64 output pins. As illustrated in Figure 3a, the FPGA provides four 16-bit ports (CF0–CF3), each driving a latching subsystem that controls 64 diodes via a decoder for selection. The routing layout on the PCB, shown in Figure 3b, uses different colors for each CF latching system for better visibility and easier identification of signal paths.

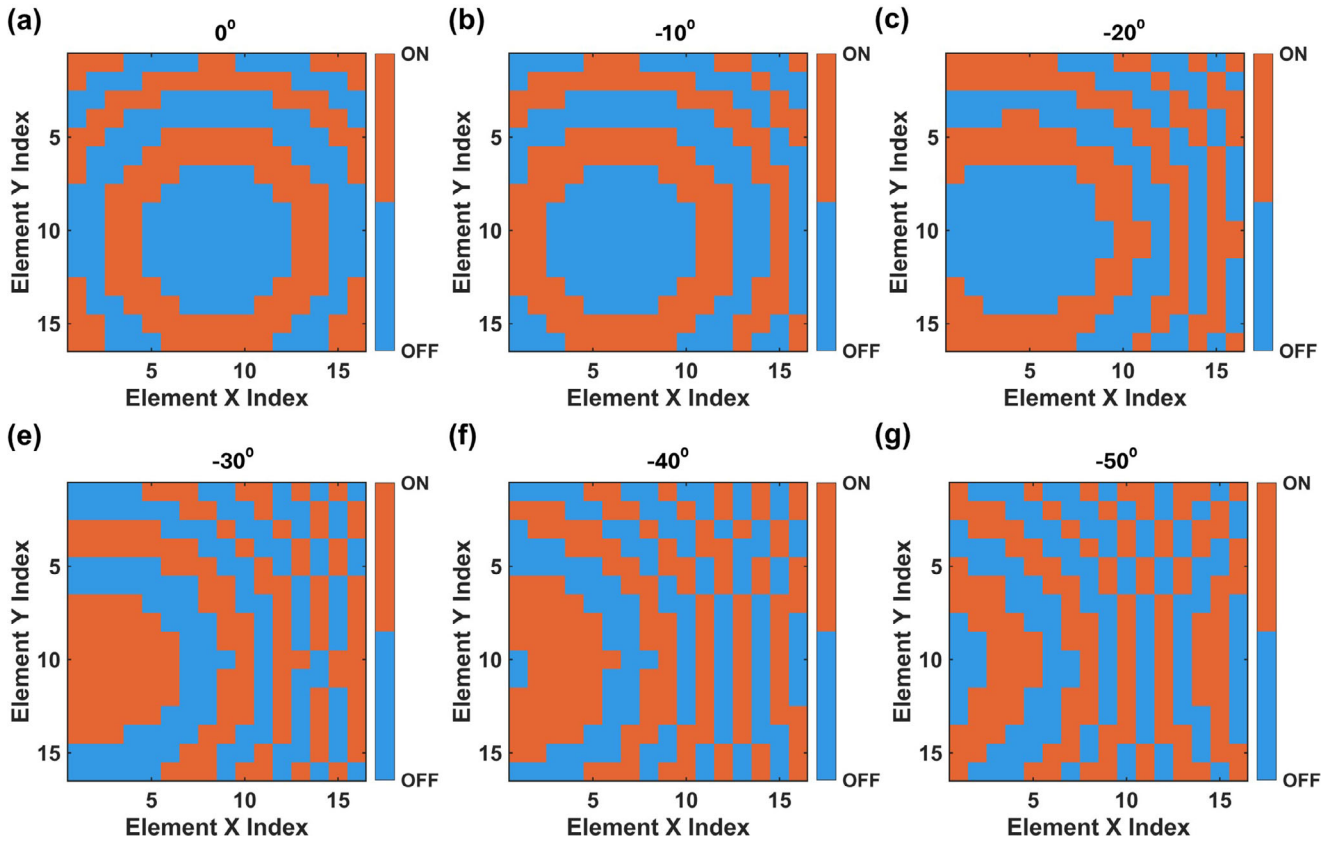


FIGURE 5 | Diodes configuration for beam steering of 16 × 16 elements RIS when F/D = 0.9, horn placement at $\phi = 15°$ and beam steering angles of 0, −10°, −20°, −30°, −40°, and −50°.

Within each CF subsystem, the 16-bit input is connected in parallel to four latches. A common two-bit input and four-bit output decoder determines, which latch updates its output, as shown in Figure 3c. When the decoder output value is n, latch $n-1$ propagates the FPGA input to the diodes through a current-limiting resistor and an LED, while the remaining latches maintain their previous states. The LED serves both as an indicator and as part of the current path, preserving the programmed diode configuration. The PCB layout showing horizontal control lines from each latch to the diodes is presented in Figure 3d.

All latching subsystems share the same decoder input, allowing the FPGA to sequentially update diode groups while maintaining parallel data transfer across the four ports. This time-multiplexing reduces the effective update rate to one quarter of the raw parallel speed, while still providing high switching performance with reduced I/O overhead. Diode control values are delivered to the FPGA through multiple interfaces, including UART (via a host computer or USB), Wi-Fi, or LAN modules integrated into the RIS PCB. We used an XC7A100T (Artix-7) device for the FPGA, SN74ACT16373Q-EP for the latches, and SN74S139AD for the decoders. For the 16×16 RIS tile, once a configuration is stored in the FPGA, the internal update is completed in approximately 40 ns. Including the external control link, the end-to-end reconfiguration time is about 40 μs when using the LAN or Wi-Fi (Ethernet-based) interfaces, and up to 100 μs when using the USB/UART serial interface.

3 | Measurements

To validate the electromagnetic performance of the fabricated RIS, two types of measurements were conducted: (i) reflection coefficient characterization of the full RIS panel, and (ii) far-field radiation pattern measurement of the complete RIS panel. All measurements were performed in a standard anechoic chamber to suppress unwanted multipath reflections.

3.1 | Reflection Response Measurements

The measurement setup schematic for characterization of the reflection coefficient is illustrated in Figure 4a. The reflection response of the RIS, shown in Figure 4b, was measured using a vector network analyzer (VNA). A standard gain horn antenna served as the transmitter (excited via port one of the VNA), illuminating the RIS prototype at an incidence angle of 10° inside the anechoic chamber. The distance between the horn and the RIS was chosen to satisfy the far-field condition based on the horn aperture size. The reflected signal was captured by a receiving horn antenna aligned at −10° for maximum power.

The transmission magnitude and phase responses were normalized using a reference aluminum plate of identical dimensions to the RIS aperture, accounting for cumulative losses in the measurement setup, including RF cable attenuation, free-space propagation loss, and return-path loss. By applying different bias states to the tunable elements (PIN diodes), distinct reflection

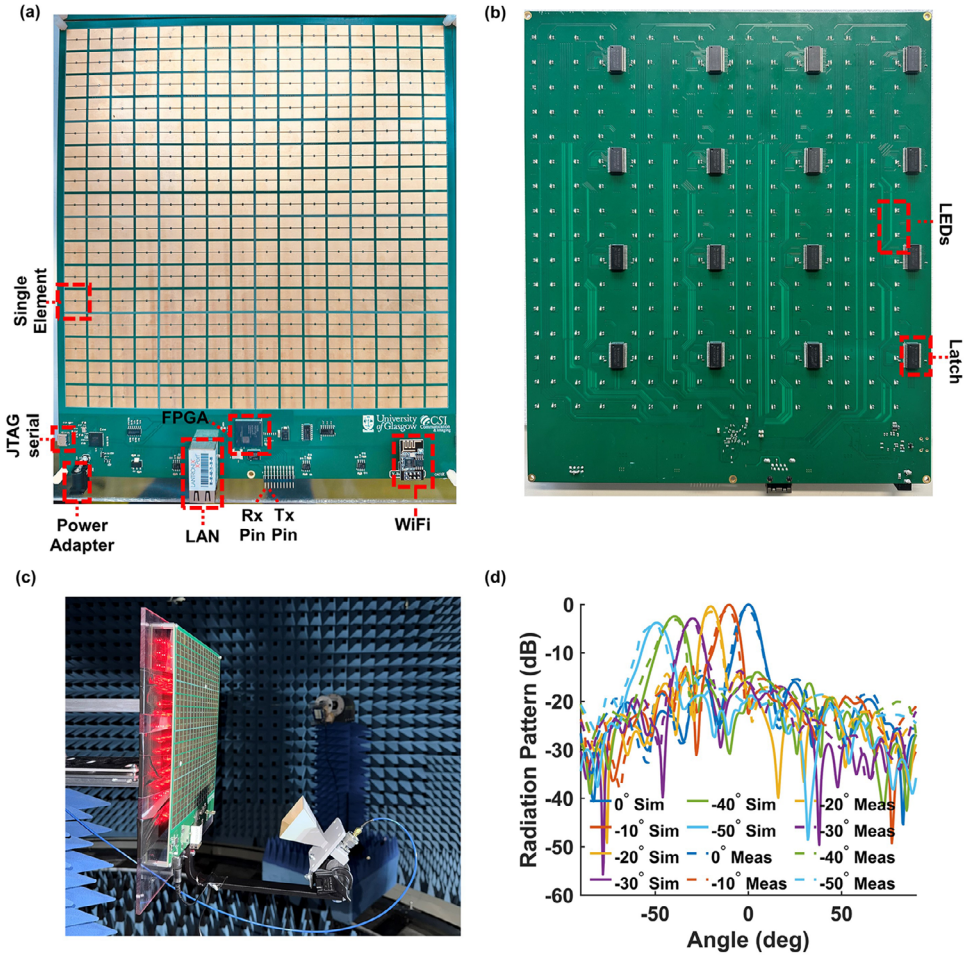


FIGURE 6 | (a) Front view of the fabricated 16 × 16 RIS tile. (b) Back view showing the integrated control PCB. (c) Near-field measurement setup inside the anechoic chamber. (d) Simulated and measured far-field radiation patterns for different steering angles.

responses were obtained, validating the reconfigurability of the RIS. The magnitude and phase of the reflection coefficient were measured for two states, namely when all diodes were OFF and when all were ON. The measurements were compared with simulation results of the UC under periodic boundary conditions at 10° incidence. The comparison analysis of reflection magnitude and phase is provided in Figure 4c,d, respectively. It is evident that the RIS prototype exhibits reflection magnitude and phase responses consistent with the simulations in the 9–10 GHz band, with only slight deviations attributable to fabrication tolerances and differences between the equivalent circuit model and actual diode behavior. Furthermore, the prototype clearly demonstrates one-bit phase reconfigurability.

3.2 | Beam Steering Measurements

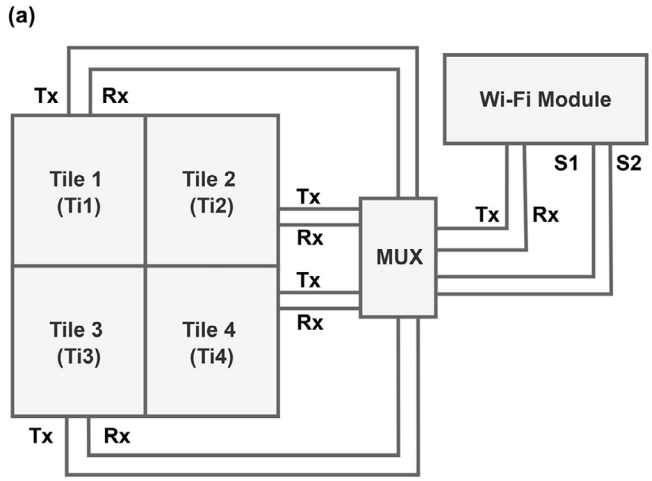
Based on the measured reflection magnitude and phase response, a 16 × 16 RIS is designed and simulated using HFSS full-wave simulation. Each UC in the RIS is integrated with a PIN diode, which is modeled using an RLC boundary, resulting in 256 PIN diodes providing phase reconfigurability. A vertically polarized horn antenna is used as an RF source and is placed at an offset angle of $\phi = 15°$ to avoid feed blockage at the RIS bore-sight. The horn antenna is placed at a distance of 23 cm, which corresponds to $F/D = 0.9$. In our case, the edge taper is around −9.5 dB, which enables optimal illumination and spillover efficiencies.

For the RIS system, the required compensation phase ϕ_{rmn} for the $(m,n)^{\text{th}}$ element is computed by

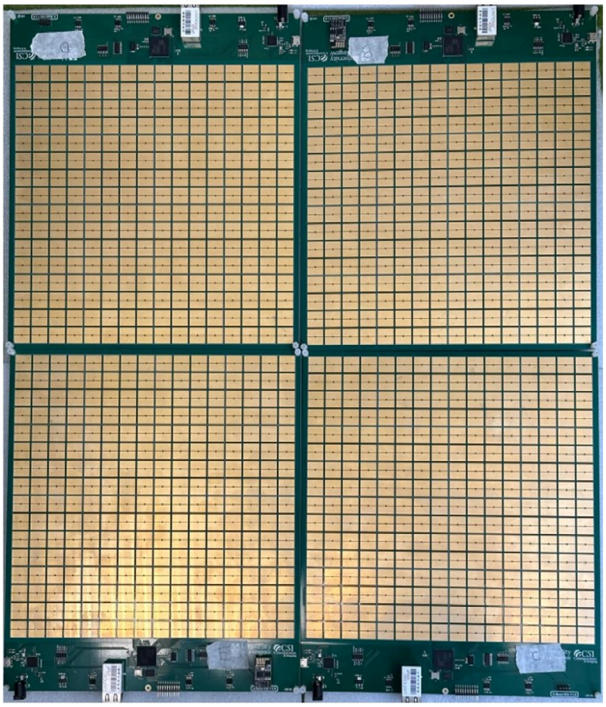
$$\phi_{rmn} = \phi_{fmn} - k \times \hat{\mu}_0 + \Delta\phi \tag{1}$$

where ϕ_{fmn} is the phase delay due to the spatial distance from the feed to the $(m,n)^{\text{th}}$ element, k denotes the free-space wavenumber, $\hat{\mu}_0$ is the unit vector in the main beam direction, and $\mathbf{r}_{mn}$ is the position vector of the $(m,n)^{\text{th}}$ element. A constant reference phase $\Delta\phi$ is added in (1) to provide additional design freedom [30, 31].

For an ideal RIS element having a continuous 360° phase range, varying $\Delta\phi$ has no effect on the phase difference between two arbitrary elements in the RIS aperture. For a one-bit RIS, however, there are only two phase states for each element, i.e., 0 and 180° in this design. If a different $\Delta\phi$ is considered, the ϕ_{rmn} of each element computed using (1) changes, and when ϕ_{rmn} is quantized, it results in different PIN states (ON or OFF), which may alter the relative phase between two arbitrary elements. In this study, we considered $\Delta\phi = 65°$ after several iterations to achieve high gain in the broadside direction. Figure 5 shows examples of diode



(b)



(c)

S1	S2	Tile
0	0	Ti1
0	1	Ti2
1	0	Ti3
1	1	Ti4

FIGURE 7 | Cascading and control of the RIS tiles: (a) cascading four tiles using a single Wi-Fi module, (b) four-tile RIS with two inverted tiles forming a 32×32 array, (c) two-bit selection mechanism using S_1 and S_2 pins for addressing each tile.

configuration for different steering directions when the horn is placed at $\phi = 20°$ and 180 mm from the RIS center.

$$\Phi_q(\phi_{rmn}) = \begin{cases} 0°, & \phi_{rmn} \in [0°, 90°] \cup [270°, 360°) \\ 180°, & \phi_{rmn} \in [90°, 270°) \end{cases}$$

Figure 6 summarizes the measurement setup and results for the fabricated RIS. The front and back views of the prototype are shown in Figure 6 ab, respectively, while Figure 6c illustrates the measurement environment inside the anechoic chamber. In this setup, the RIS is characterized using a spherical near-field scanning system, where the probe measures the E-field amplitude and phase over a defined spherical surface. The recorded near-field data are then converted into far-field radiation patterns using a standard near-field-to-far-field (NF–FF) transformation algorithm. The ON-OFF configurations based on the phase profiles in Figure 5 were implemented using the integrated WiFi module, and can also be updated via LAN or USB serial port. The tile ON-OFF configuration can be updated in less than 10 ms. The measured far-field radiation patterns are shown in Figure 6d and compared with the simulation results. For consistent comparison across steering angles, all patterns are normalized with respect to the maximum simulated broadside gain of 20.8 dBi. The measured peak gain is 20.2 dBi at the broadside $\theta = 0°$ and decreases to 18.2 dBi at the peak steering angle of $\theta = \pm 50°$. It is clear that a good correlation is observed across the main lobe direction and beamwidth with only minor deviations in sidelobe levels, which can be attributed to fabrication tolerances and finite measurement resolution. Overall, the consistency between simulation and measurement confirms the accuracy of the proposed design methodology and validates the beamforming capability of the fabricated RIS.

4 | RIS Scalability

As explained earlier, a single RIS tile consists of a 16×16 UC. We extended this design to a 32×32 RIS by cascading four 16×16 tiles. Figure 7a illustrates the cascading process and the management of the ON/OFF configuration of diodes in each tile. To form a square-shaped 32×32 RIS, two of the tiles are physically inverted, as shown in Figure 7b. Alternatively, the tiles can be cascaded linearly, allowing construction of arbitrarily large rectangular apertures. Cascading vertically is constrained because the lower section of the prototype houses SMD devices, including WiFi and LAN modules, which could introduce undesired reflections if additional tiles are added.

Each tile can be independently controlled through its integrated LAN, USB, or WiFi module. Additionally, the entire RIS can be operated collectively via a single WiFi interface. As shown in Figure 6a, 20-pin male connectors are integrated per tile: two pins handle data transmission and reception, while the remaining pins supply power and ground. A $four$-input multiplexer (MUX) is employed, with two pins dedicated to TX/RX data and two selection pins (S_1, S_2) to address the desired tile. The selection mechanism, summarized in the table within Figure 7c, defines how each tile's ON/OFF states are updated sequentially through the single WiFi module. The total power consumption of the full 32×32 RIS was measured under multiple switching states.

The consumption was 8.25 W when all diodes were OFF, 13 W when all diodes were ON, and 11.25–11.60 W during beam-steering operation.

5 | Conclusion

A scalable X-band reconfigurable intelligent surface (RIS) with one-bit phase-tunable unit cells has been presented and experimentally validated. The proposed unit cell, integrating a PIN diode into a slotted copper patch, achieves a phase shift of 180° ± 20° across 9–10 GHz. A 16×16 RIS demonstrates high gain and effective beam steering, achieving 20.5 dBi at broadside and 18.6 dBi at $\theta = \pm 50°$. Both the reflection characteristics and beam steering capability of the RIS were measured in a near-field setup and compared with full-wave simulations, showing good agreement. The RIS enables fast reconfiguration with update times below 10 ms via FPGA, and supports multiple control interfaces, including LAN, USB, and WiFi. Scalability is confirmed through a four-tile prototype, where each tile can be independently controlled or coordinated via a single WiFi module, allowing flexible and self-contained operation. The results validate that the proposed RIS architecture provides a practical and scalable solution for beam-steering applications with reliable and predictable performance. These results demonstrate the potential of the presented architecture to serve as a building block for large-area intelligent surfaces and adaptive wireless links, where scalable, low-cost, and reconfigurable control is essential for dynamic beam management and environment-aware communication.

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Conflicts of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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